66-

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

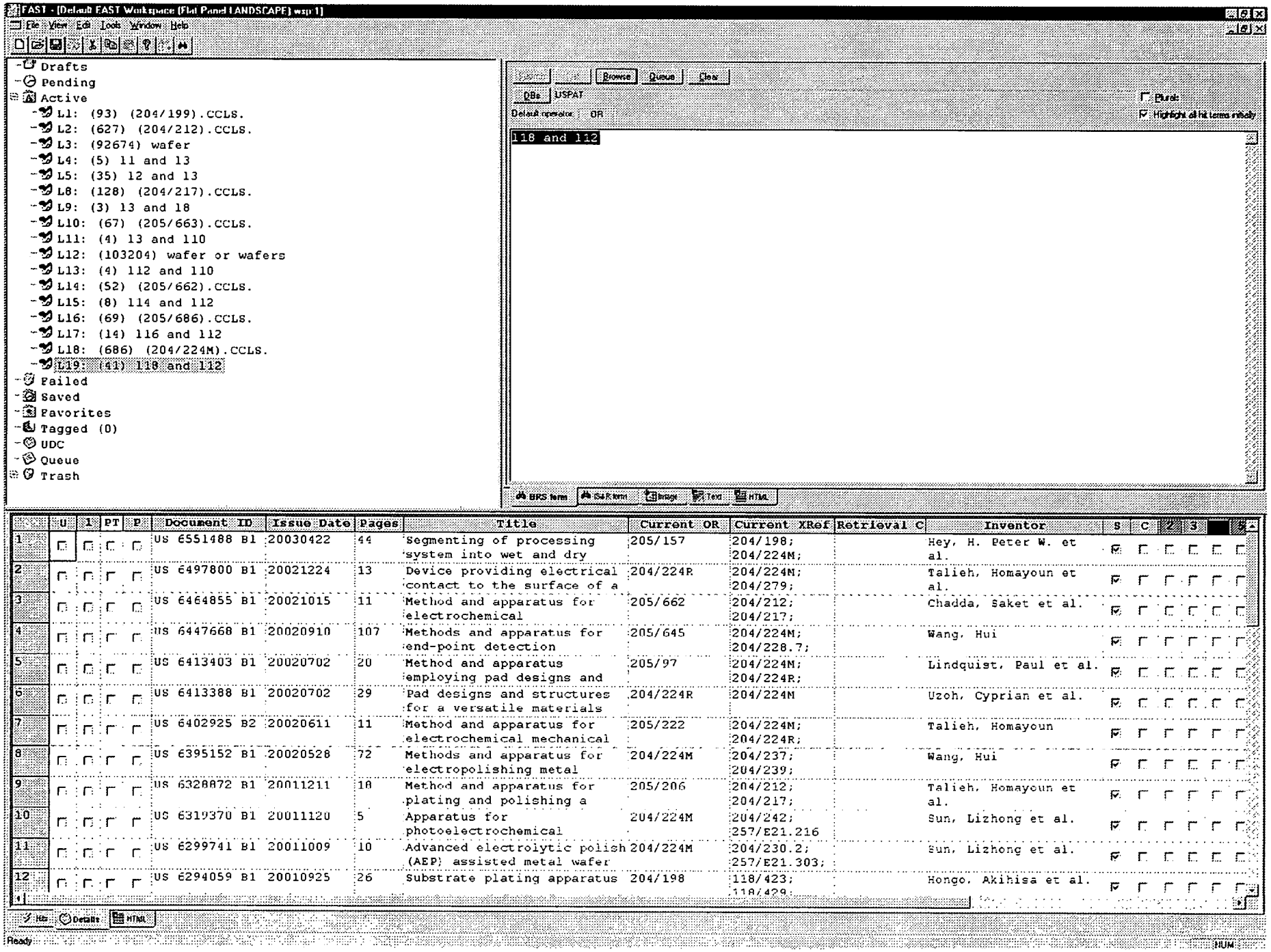
Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.



	U	1	PT	P	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	2	3
1	☐	☐	☐	☐	US 6551488 B1	20030422	44	Segmenting of processing system into wet and dry	205/157	204/198; 204/224M;		Hey, H. Peter W. et al.	☑	☐	☐	☐
2	☐	☐	☐	☐	US 6497800 B1	20021224	13	Device providing electrical contact to the surface of a	204/224R	204/224M; 204/279;		Talieh, Homayoun et al.	☑	☐	☐	☐
3	☐	☐	☐	☐	US 6464855 B1	20021015	11	Method and apparatus for electrochemical	205/662	204/212; 204/217;		Chadda, Saket et al.	☑	☐	☐	☐
4	☐	☐	☐	☐	US 6447668 B1	20020910	107	Methods and apparatus for end-point detection	205/645	204/224M; 204/228.7;		Wang, Hui	☑	☐	☐	☐
5	☐	☐	☐	☐	US 6413403 B1	20020702	20	Method and apparatus employing pad designs and	205/97	204/224M; 204/224R;		Lindquist, Paul et al.	☑	☐	☐	☐
6	☐	☐	☐	☐	US 6413388 B1	20020702	29	Pad designs and structures for a versatile materials	204/224R	204/224M		Uzoh, Cyprian et al.	☑	☐	☐	☐
7	☐	☐	☐	☐	US 6402925 B2	20020611	11	Method and apparatus for electrochemical mechanical	205/222	204/224M; 204/224R;		Talieh, Homayoun	☑	☐	☐	☐
8	☐	☐	☐	☐	US 6395152 B1	20020528	72	Methods and apparatus for electropolishing metal	204/224M	204/237; 204/239;		Wang, Hui	☑	☐	☐	☐
9	☐	☐	☐	☐	US 6328872 B1	20011211	18	Method and apparatus for plating and polishing a	205/206	204/212; 204/217;		Talieh, Homayoun et al.	☑	☐	☐	☐
10	☐	☐	☐	☐	US 6319370 B1	20011120	5	Apparatus for photoelectrochemical	204/224M	204/242; 257/E21.216		Sun, Lizhong et al.	☑	☐	☐	☐
11	☐	☐	☐	☐	US 6299741 B1	20011009	10	Advanced electrolytic polish (AEP) assisted metal wafer	204/224M	204/230.2; 257/E21.303;		Sun, Lizhong et al.	☑	☐	☐	☐
12	☐	☐	☐	☐	US 6294059 B1	20010925	26	Substrate plating apparatus	204/198	118/423; 118/429		Hongo, Akihisa et al.	☑	☐	☐	☐

4/2003

EAST Browser - L5: (35) 2 and 3 | US 6464855 B1 | Tag: S | Doc: 6/35 (SORTED) | Format: KWIC

File Edit View Tools Window Help

	Document ID	Pages	1	2	3	4	5	U	S	C	P	Kind Codes	Sou
1	US 6551484 B2	46							☑				USPAT
2	US 6544391 B1	14							☑				USPAT
3	US 6500316 B1	8							☑				USPAT
4	US 6478937 B2	29							☑				USPAT
5	US 6478936 B1	17							☑				USPAT
6	US 6464855 B1	11							☑				USPAT
7	US 6454916 B1	8							☑				USPAT

US-PAT-NO: 6464855

DOCUMENT-IDENTIFIER: US 6464855 B1

TITLE: Method and apparatus for electrochemical planarization of a workpiece

---------- KWIC ---------

Brief Summary Text - BSTX (2):

The present invention relates, generally, to systems for polishing or planarizing workpieces, such as semiconductor wafers. More particularly, it relates to an apparatus and method for electrochemical planarization of a wafer having a metallized surface.

Brief Summary Text - BSTX (4):

The production of integrated circuits begins with the creation of high-quality semiconductor wafers. During the wafer fabrication process, the wafers may undergo multiple masking, etching, and dielectric and conductor deposition processes. In addition, metallization, which generally refers to the materials, methods and processes of wiring together or interconnecting the component parts of an integrated circuit located on the surface of a wafer, is critical to the operation of a semiconductor device. Typically, the "wiring" of an integrated circuit involves etching trenches, or "vias", in a planar dielectric (insulator) layer and filling the trenches with a metal.

Brief Summary Text - BSTX (5):

In the past, the primary metallization material used in semiconductor fabrication was aluminum due to the leakage and adhesion problems experienced with the use of gold and the high contact resistance with silicon experienced with copper. Other metallization materials have included Ni, Ta, Ti, W, Ag, Cu/Al, TaN, TiN, CoWP, NiP and CoP. Over time, the semiconductor industry has slowly been moving to the use of copper for metallization due to the alloying and electromigration problems that are seen with aluminum. When copper is used as the filling, typically a barrier layer of another material is first deposited to line the trenches and vias to prevent the migration of copper into the dielectric layer. Barrier metals may be W, Ti, TiN, Ta, TaN, various alloys, and other refractory nitrides, which may be deposited by CVD, PPD, or electroless or electrolytic plating. To achieve good fill of the trenches and vias, extra metal is deposited in the process, such metal covering areas of the wafer above and outside the trenches and vias. After filling, planarization is typically conducted to remove the extra metal down to the dielectric surface. Planarization leaves the trenches and vias filled and results in a flat, polished surface.

Brief Summary Text - BSTX (6):

Because of the high precision required in the production of integrated circuits, an extremely flat surface is generally needed on at least one side of the semiconductor wafer to ensure proper accuracy and performance of the

(12) **United States Patent**
Chadda et al.

(10) **Patent No.: US 6,464,855 B1**
(45) **Date of Patent: Oct. 15, 2002**

(54) **METHOD AND APPARATUS FOR ELECTROCHEMICAL PLANARIZATION OF A WORKPIECE**

(75) Inventors: **Saket Chadda**, Phoenix, AZ (US); **Chris Berns**, Portland, OR (US)

(73) Assignee: **SpeedFam-IPEC Corporation**, Phoenix, AZ (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 50 days.

(21) Appl. No.: **09/679,473**

(22) Filed: **Oct. 4, 2000**

(51) **Int. Cl.**[7] **C25F 3/16**; C25F 7/00; C25D 17/00

(52) **U.S. Cl.** ..... **205/662**; 205/663; 205/686; 204/224 M; 204/212; 204/217

(58) **Field of Search** ..... 205/662, 663, 205/686; 204/224 M, 217

(55) **References Cited**

U.S. PATENT DOCUMENTS

3,959,089	A *	5/1976	Watts	204/217 X
5,256,565	A	10/1993	Bernhardt et al.	
5,567,300	A	10/1996	Datta et al.	
5,863,412	A	1/1999	Ichinose et al.	
5,993,537	A	11/1999	Hisamatsu et al.	
6,017,437	A	1/2000	Ting et al.	
6,056,869	A	5/2000	Uzoh	
6,077,412	A	6/2000	Ting et al.	
6,171,467	B1 *	1/2001	Weihs et al.	204/224 R
6,176,992	B1	1/2001	Talieh	
6,299,741	B1 *	10/2001	Sun et al.	204/224 M
6,328,872	B1 *	12/2001	Talieh et al.	205/206

FOREIGN PATENT DOCUMENTS

GB	2 069 531	8/1981
WO	WO00/26443	5/2000

OTHER PUBLICATIONS

Robert J. Contolini, Anthony F. Bernhardt and Steven T. Mayer, *Electrochemical Planarization for Multilevel Metallization*, J. Electrochem. Soc., vol. 141, No. 9 (No Date).

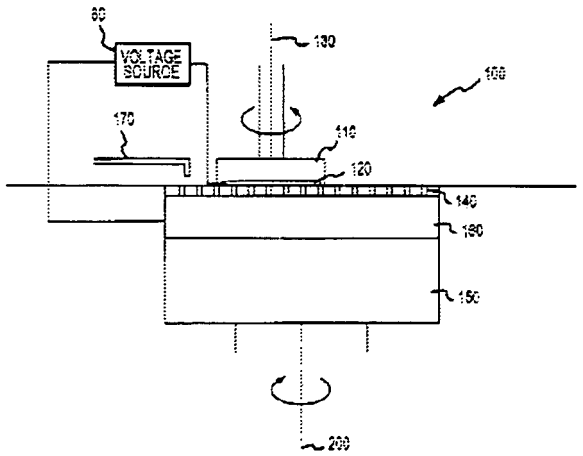
* cited by examiner

Primary Examiner—Donald R. Valentine
(74) *Attorney, Agent, or Firm*—Snell & Wilmer, LLP

(57) **ABSTRACT**

An electrochemical planarization apparatus for planarizing a metallized surface on a workpiece includes a platen, a conductive element disposed adjacent the platen and a polishing surface disposed adjacent the conductive element. A workpiece carrier is configured to carry a workpiece and press the workpiece against the polishing surface while causing relative motion between the workpiece and the polishing surface. A voltage source is configured to effect an electric potential difference between the metallized surface on the workpiece and the conductive element so that an electric field is produced between the metallized surface and the conductive element. The apparatus further includes a solution application mechanism configured to supply an electrolytic solution to the polishing surface.

27 Claims, 5 Drawing Sheets



4/2003

FAST Browser - L19: (41) 18 and 12 | US 6413403 | Tag: 5 | Doc: 5/41 (SORTED) | "Full" 17/20 (Total images 20)

File Edit View Tools Window Help

	Document ID	Pages	1	2	3	4	5	6	U	S	C	P	Kind Codes	Sou
1	US 6551488 B1	44												USPAT
2	US 6497800 B1	13												USPAT
3	US 6464855 B1	11												USPAT
4	US 6447668 B1	107												USPAT
5	US 6413403 B1	20												USPAT
6	US 6413388 B1	29												USPAT
7	US 6402925 B2	11												USPAT

US-PAT-NO: 6413403

DOCUMENT-IDENTIFIER: US 6413403 B1

TITLE: Method and apparatus employing pad designs and structures with improved fluid distribution

---------- KWIC ---------

Detailed Description Text - DETX (3):

The present invention can be used to deposit and/or remove materials on any substrate, such as a wafer, flat panel, magnetic film head, integrated circuit, package, semiconductor device or chip, or any other device or workpiece of interest. For purposes of this description, the terms "substrate" and "workpiece" can be used interchangeably. Further, the specific parameters referred to herein, such as materials, dimensions, thicknesses, and the like, are intended to be explanatory rather than limiting.

Current US Cross Reference Classification - CCXR (1):

205/224X

bubbles to escape and prevents their accumulation over the anode **406**. It also allows for the selective loss of anode sludge material in the case of soluble anode materials like CuP, where thick anode sludge may affect metal deposit uniformity. Thus, in this arrangement, the volume of electrolyte E1 at any given time discharged into the anode chamber **452** is such that

$$E1=E2+E4,$$

where E2 is the allowed controlled leakage volume to help purge bubbles and anode fines, and the balance E4 is the portion filtered through filter **454** and migrated to the substrate surface via the pad support member channels and pad channels.

Preferably, the amount of solution E2 allowed to leak ranges between about 0.1 to 20%, but preferably between about 1 to 10% of the total electrolyte flow E1. Also, it is preferred that the volume E4 of the electrolyte discharged into the anode chamber to minimize concentration polarization ranges between about 10 to 40%, but preferably between about 15 to 30% of the volume flow. Thus, the orifices in the shaft **450** discharging E1 into the anode chamber **452** may be chosen accordingly.

In FIG. **4***b*, the anode **406** resides or is secured in anode housing **460**. A clearance gap **93** separates the anode housing **460** from portions of the pad support chamber adjacent to it. This clearance gap **93** is configured to allow for the controlled electrolyte leak **E2** in this region as described earlier. Besides the clearance gap, tiny holes (not shown), typically less than 0.5 mm in diameter, may be drilled around the top of the anode housing **460** to supplement the clearance gap to manage the controlled leak. One or more large ports may also be secured to this region to control the leak solution volume **E2**.

The electrolyte E3 emanating from the substrate and the controlled leakage solution E2 may drain through a drain opening **462** at the bottom of the anode chamber **405**. These solutions are typically drained to a reservoir for process filtering, and then recycled back to the deposition chamber. Also in FIG. **4***b*, as described earlier, the pad support member **420** may rotate. In this configuration, the anode housing **460** remains stationary. Electrolyte solution injected into the anode chamber **405** from a stationary or rotating pad support member causes excellent agitation of the electrolyte in the anode chamber **405**. The rotation of the pad support member **420** may range from about 3 to 400 rpm, but preferably between about 5 to 300 rpm. It is again to be understood that the support member electrolyte channel, distribution channel and pad electrolyte channel combinations according to the invention are to take the place of (a) the electrolyte channels in the support member **420** of FIG. **4***b*, and (b) corresponding electrolyte channels in the pad material **430** in FIG. **4***b*. Once again, additional channels providing for predominantly electric field communication could be included in the pad.

Referring again to FIG. **4***a*, an example involving copper deposition will be described. A suitable copper plating solution is circulated from a reservoir through the lower chamber **404** from electrolyte inlet **408**. The anode **406** may rotate to help the expulsion of flow of the electrolyte from the lower chamber **404** to the upper chamber **407** via the channels in the pad support member **422** and the channels in the pad material **430**. Electrolyte flow may range between about 50 ml/min to about 12 L/min, but preferably between about 100 ml/min to 5 L/min depending on the size of the substrate **10**. The larger the substrate size, the higher the flow rate. As the fluids emanate through and wetten the pad

430, the substrate **10** is lowered to rotate, glide or hydroplane on the surface of the wet pad **430**.

The anode and cathode may be energized after a brief moment of wetting the substrate. The current density in the cathode may range between about 1 to 50 mA/cm^2, but preferably between about 5 to 45 mA/cm^2.

For example, the substrate may be plated at a current density of about 10 to 25 mA/cm^2 for 20 to 70% of the deposition time at a pressure of about 0 to 0.5 psi, and at a higher pressure for the 30 to 80% balance of the deposition time. The pressure on the substrate may increase from 0 to 0.5 psi mentioned above to 0.5 to 3 psi. The electrolyte flow may also be varied within the intervals. Also during the deposition, the carrier head may make continuous or intermittent contact with the stationary pad or rotating pad. The substrate and the anode may rotate between about 2 to 250 rpm, but preferably between about 5 to 200 rpm. Also, lateral movement of the substrate relative to the pad may occur during the deposition process. The speed of the lateral motion may ranges between about 0.5 to 25 mm/second.

The lateral motion is programmed such that the substrate, while rotating, comes to rest momentarily at various points, or during any stage of its motion. In addition, the rotation of the substrate may be varied in such a manner that, for instance, the substrate is rotated at only about 50 to 85% of normal when the substrate is at one end of a smaller anode/pad than when the centers of the substrate and anode coincide.

Also, the pressure on the substrate is varied depending on the later position of the substrate relative to the pad. Thus, for a given pad design, the combination of various lateral motions, substrate rotation, substrate pressure and electrolyte flow rate may be used to control the uniformity of the deposited material. The deposited material may be either uniform or thinner at the edge or center of the substrate. Using the above process and an appropriate electrolyte, a superplanar metal deposit may be readily obtained when copper or any other metal is deposited over structures of the type shown in FIG. **1***a*. A resulting superplanar deposition structure is shown in FIG. **2***c*, in which the material overburden across the substrate is nearly independent of the width of the features on the substrate. This contrasts with deposited material structures from conventional metal deposition systems as shown in FIG. **1***c*.

The apparatus of FIGS. **4***a* and **4***b* can also be used for etching. Using a shaped pad in which only a small quadrant or rectangular area is accessible to the electrolyte and the electric field, the substrate may be electro-polished or electro-etched in a very controlled manner. The difficulty with electro-etching using a standard pad is that because electric current flows from the substrate's edge towards its center, the material removal rate is higher closer to the electrical contacts. Hence, by making the pad holes or channel openings arranged closer to the contacts smaller in diameter and fewer in number than those towards the center of the pad, the rate of metal removal by wet etch, electro-etching or polish may be rendered uniform from the center to the edge of the substrate, or may be dynamically controlled.

The apparatus allows for the deposition/removal of material on a substrate or workpiece surface while the surface is in static or dynamic contact with another surface. The other surface need not be the anode. The workpiece surface may be abrasive or non-abrasive in nature. It is essential, however, that the material of the other surface transmit fluid or electrolytes between an anode and a workpiece, as well as allow magnetic, electric or electromagnetic fields to com-

w/1315 pad may be abrasive

FAST Browser - L19 (41) 18 and 12 | US 6413403 B1 | Tag: S | Doc: 5/41 (SORTED) | Format: KWIC

File Edit View Tools Window Help

	Document ID	Pages	1	2	3	4	5	U	S	C	P	Kind Codes	Sou
1	US 6551488 B1	44											USPAT
2	US 6497800 B1	13											USPAT
3	US 6464855 B1	11											USPAT
4	US 6447668 B1	107											USPAT
5	US 6413403 B1	20											USPAT
6	US 6413388 B1	29											USPAT
7	US 6402925 B2	11											USPAT

US-PAT-NO: 6413403

DOCUMENT-IDENTIFIER: US 6413403 B1

TITLE: Method and apparatus employing pad designs and structures with improved fluid distribution

---------- KWIC ---------

Detailed Description Text - DETX (3):

The present invention can be used to deposit and/or remove materials on any substrate, such as a wafer, flat panel, magnetic film head, integrated circuit, package, semiconductor device or chip, or any other device or workpiece of interest. For purposes of this description, the terms "substrate" and "workpiece" can be used interchangeably. Further, the specific parameters referred to herein, such as materials, dimensions, thicknesses, and the like, are intended to be explanatory rather than limiting.

Current US Cross Reference Classification - CCXR (1):

204/224R

cal Mechanical Deposition", the specification of which is incorporated by reference herein as non-essential matter.

In FIG. 3a, an anode component, generally indicated at 322, includes a bottom portion 322a, which may be a soluble or inert anode material, attached to an anode holder or housing 322b by known methods. A stiff upper pad support member 320 is attached or secured to the anode holder 322b. Electrically isolating the anode holder 322b from the stiff pad support member 320 is an insulating spacer 322c.

The pad support member 320 is secured to the anode holder 322b with screws in a manner such that they are both electrically isolated from one another. An electrolyte or solution chamber 322e is therefore formed between anode bottom portion 322c and the pad support member 320. The gap 322f separates the anode bottom portion 322a from the pad support member 320. Small channels 324 are formed in the pad support member 320 for fluid solutions to communicate between the chamber 322e to the substrate 10. A polishing pad material 330 is attached above the pad support member 320. The polishing pad material 330 may contain two or more distinct types of channels. Channels 330a are provided for the fluids to communicate between the chamber 322e and the substrate 10, and channels 330b are provided for mostly an electric field to communicate between the anode bottom portion 322a, via the electrolyte chamber 322e and pad support member 320, and the substrate 10. The combination of channels (sometimes referred to as holes) is used to manipulate the electrolyte fluid flow and electric field distribution over the substrate 10 to control the nature of the material deposited on the substrate, in particular the uniformity of the deposit on the substrate.

The pad material 330 is secured to the pad support member 320 with the aid of a fastener, such as an adhesive material 332. The entire anode bottom portion-pad support member-pad assembly 322 is housed in another chamber 334, in which electrolytes emanating from interface 334b between the substrate 10 and a surface of the pad material 330 accumulate. This accumulated electrolyte solution may be pumped into a reservoir system for reclamation and reuse, or may just simply be discarded.

It is further noted that electrical contact with the anode bottom portion 322a may occur directly or via the anode housing 322b, while another electrical contact of opposite polarity is made to the substrate 10. Thus, electrical contact need not be made to the pad support member 320.

By way of example, the anode housing 322b may be formed of polymeric material such as PVDP, polypropylene, PTFE, and/or other materials that are essentially inert to the electrolyte fluids used in the reaction. However, it is most preferred that the anode housing 322b be made of titanium, stainless steel, graphite, and the like. The anode housing may also be coated with a very thin layer of platinum or palladium. The anode material itself may be an inert type of anode such as graphite, platinized metals, such as Pt/Ti, and the like. In some inert anode applications, for simplification, the inner wall of the anode housing 322b may serve as the anode.

In other applications, a soluble anode 322a may be housed in the anode housing 322b. Copending and commonly assigned U.S. application Ser. No. 09/568,584, titled ANODE ASSEMBLY FOR PLATING AND PLANARIZING A CONDUCTIVE LAYER, filed May 11, 2000, discloses the use of a soluble or consumable anode. The soluble anode 322a may be formed by materials such as Cu, phosphorized Cu, Ni, gold, Pt, Ag, Cd, Rh and/or various other alloy electrode materials depending upon the material

to be plated. The insulating sealing spacer 322c may be made of a polymeric material or a combination of polymeric/metallic and/or polymeric/ceramic materials. It is only essential that the electrolyte or fluids used in the reaction do not degrade the spacer 322c, and/or that the spacer 322c does not adversely affect the designed qualities of the metal deposited on the substrate 10. Additionally, the method of securing the pad support member 320 via the insulating spacer 322c must not electrically short the anode 322a to the pad support member 320.

The pad support member 320 is preferably fabricated from a stiff material with a very specific modulus, such as carbon, titanium and the like. Stainless steel may also be used. The pad support member material must not interact in an adverse manner with the deposition fluids so as to affect the material deposited on the substrate. The thickness of the pad support member 320 is such that the member behaves as if it has an infinite stiffness relative to itself (weight) and with respect to the applied polishing load. Additionally, the pad support member 320 may be coated with a very thin layer of platinum or palladium, e.g. about up to 500 Å, to enhance the adhesion of the pad material 330 and also to enhance the electric field dispersion.

The anode housing 322b of FIG. 3a has at least one channel for fluid entry (not shown) such that the electrolyte fluid can fill the chamber 322e formed by the gap 322f. The electrolytes then pass through the small channels or holes 324, 324b in the pad support member 320 and through the channels or holes 330a in the pad material 330 to a surface of the substrate 10. The fluid exits the substrate surface as indicated at 334b and returns to the bottom of the outer chamber housing 334, where it is drained via drain opening 334c.

Referring back to the channels or holes formed in the pad material 330, more than one type of channel/hole with respect to the pad support member 320 or the anode 322a may be provided. For example, a first family of channels 330a (or holes, cavities, etc.) can be designed and positioned for fluid and electric field transfer from the electrolyte chamber 322e to the substrate. Hence, the channels 330a may be disposed directly on, or adjacent to, channels 324b formed in the pad support member 320 as shown in FIG. 3a. Another family of holes or channels 330b is positioned, with respect to the pad support member 320 (e.g., with the aid of the adhesive sheet 332), such that the electric field predominately communicates from the anode chamber 322e to the substrate 10 through these channels. Other channels may also be designed into the pad material 330 to enhance fluid shearing, mass transfer, and the like, at the substrate surface.

FIG. 3b is an enlarged view of the anode component of FIG. 3a showing a configuration of channels in the pad material 330. Here, the broken arrows indicate channels 330b designed for mostly electric field communication, while the solid arrows indicate channels 330a designed for mostly fluid communication. Thus, as shown by the solid/broken arrows, portions of the channels in the pad material 320 allow both the fluid and the electric field to communicate from the anode chamber 332e to the substrate. Other portions of the pad material predominantly allow the electric field to communicate as opposed to the electrolyte fluid.

Combination of these families of channels 330a, 330b and placement of adhesive sheets 332 are used to control electrolyte and electric field distribution on the substrate 10, and thus control the nature of the material deposited. More particularly, the uniformity of the deposited material can be controlled during plating or plating/polishing operations.

EAST Browser - [5: (35) 2 and 3 [US 6454916 | Tag: S | Doc: 7/35 (SORTED)] | "Full" 1/8 (Total images 8)]

File Edit View Tools Window Help

	Document ID	Pages	1	2	3	4	U	S	C	P	Kind Codes	Sou
2	US 6544391 B1	14						☑				USPAT
3	US 6500016 B1	8						☑				USPAT
4	US 6478937 B2	29						☑				USPAT
5	US 6478936 B1	17						☑				USPAT
6	US 6464855 B1	11						☑				USPAT
7	US 6454916 B1	8						☑				USPAT
8	US 6436249 B1	64					☑					USPAT

US-PAT-NO: 6454916

DOCUMENT-IDENTIFIER: US 6454916 B1

TITLE: Selective electroplating with direct contact chemical polishing

---------- KWIC ----------

Abstract Text - ABTX (1):

A deposition tool and a method for depositing a material within the recesses in a substrate of semiconductor wafer employs a rotatable diffuser that diffuses the plating material onto the top surface of a substrate. The diffuser is placed into contact with the semiconductor wafer and rotated while the plating material is applied through apertures in the diffuser. The plating material fills recesses patterned into the substrate of the semiconductor wafer but is prevented from forming to a significant degree on the top surface of the semiconductor wafer due to the contact and rotation of the diffuser. Since the plating material is not deposited on the top surface of the semiconductor wafer to any significant degree, chemical mechanical polishing (CMP) planarization is significantly reduced or completely eliminated.

Brief Summary Text - BSTX (15):

After the copper has been deposited, either by electroless deposition or by electroplating, a relatively thick layer of copper is typically formed over the top surface of the substrate, such as the dielectric layer. Although the recesses, including trenches and via holes, are typically filled with the conductive material, (e.g., copper), the excess material needs to be removed from the top surface of the substrate prior to further processing of the wafer. A commonly used method of removing the excess copper material and planarizing the copper is known as chemical-mechanical polishing (CMP) planarization. In conventional CMP processing, a reactive agent in a slurry reacts with the surface of the layer to be polished, and the abrasive particles mechanically remove the reacted surface layer. The interaction of the polishing pad abrasive particles, and reactive agent with the layer to be polished results in a polishing. Typically, a wafer is held by a carrier head with the top surface of the wafer pressed face down against the outer surface of a polishing pad. A common two-layer polishing pad, with the upper layer composed of IC-1000 the lower layer composed of SUBA-4, is available from Rodell, Inc, located in Newark, Del. (IC-1000 and SUBA-4 are product names of Rodell, Inc.).

Brief Summary Text - BSTX (19):

This and other needs are met by embodiments of the present invention which provide a method of depositing a material by electrochemical plating within recesses in a substrate of a semiconductor. In the method, a diffuser is positioned above a top surface of a substrate of a semiconductor wafer so that the diffuser contact surface is in contact with the substrate top surface. The diffuser has apertures through which flows the material to be deposited within the recesses in the substrate. The diffuser is supplied with the material to be deposited. The diffuser is rotated with respect to the top surface of the substrate of the semiconductor wafer while the diffuser is in contact with the

(12) **United States Patent**
Wang et al.

(10) **Patent No.: US 6,454,916 B1**
(45) **Date of Patent: Sep. 24, 2002**

(54) **SELECTIVE ELECTROPLATING WITH DIRECT CONTACT CHEMICAL POLISHING**

(75) Inventors: **Fei Wang**, San Jose, CA (US); **Steven C. Avanzino**, Cupertino, CA (US); **Darrell M. Erb**, Los Altos, CA (US)

(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/477,810

(22) Filed: **Jan. 5, 2000**

(51) Int. Cl.[7] **C25D 17/00**
(52) U.S. Cl. ..... **204/224 R**; 204/212
(53) Field of Search ..... 437/225; 204/224 R, 204/212

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,789,648 A		12/1988	Chow et al.	437/225
4,921,583 A	*	5/1990	Sewell et al.	204/15
5,574,787 A		10/1997	Zhao et al.	437/230
6,027,630 A	*	2/2000	Cohen	205/135
6,027,631 A	*	2/2000	Broadbent	205/137
6,099,712 A	*	8/2000	Ritzdorf et al.	205/123
6,174,425 B1	*	1/2001	Simpson et al.	205/96
6,254,742 B1	*	7/2001	Hanson et al.	204/279
6,261,426 B1	*	7/2001	Uzoh et al.	204/224 R

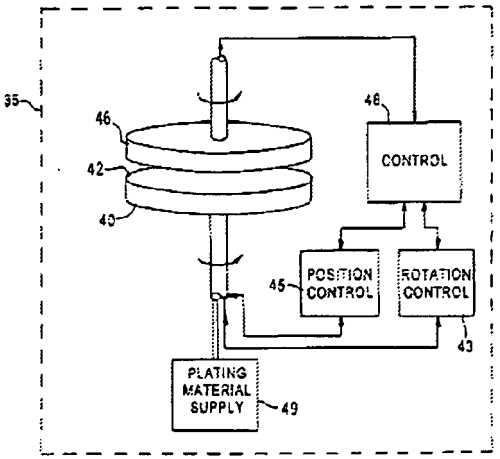
* cited by examiner

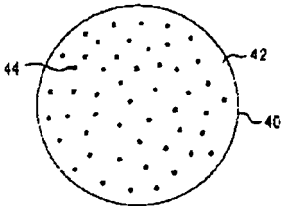
Primary Examiner—Donald R. Valentine
Assistant Examiner—Erica Smith-Hicks

(57) **ABSTRACT**

A deposition tool and a method for depositing a material within the recesses in a substrate of semiconductor wafer employs a rotatable diffuser that diffuses the plating material onto the top surface of a substrate. The diffuser is placed into contact with the semiconductor wafer and rotated while the plating material is applied through apertures in the diffuser. The plating material fills recesses patterned into the substrate of the semiconductor wafer but is prevented from forming to a significant degree on the top surface of the semiconductor wafer due to the contact and rotation of the diffuser. Since the plating material is not deposited on the top surface of the semiconductor wafer to any significant degree, chemical mechanical polishing (CMP) planarization is significantly reduced or completely eliminated.

8 Claims, 3 Drawing Sheets





FAST Browser - I.S. (35) 2 and 3 | US 6328872 | Tag: S | Doc: 12/35 (SORTED) | "Full" 1/18 (Total images 18)

File Edit View Tools Window Help

	Document ID	Pages	1	2	3		U	S	C	P	Kind Codes	Sou
7	US 6454916 B1	8										USPAT
8	US 6436249 B1	64										USPAT
9	US 6416647 B1	27										USPAT
10	US 6365017 B1	21										USPAT
11	US 6334937 B1	27										USPAT
12	US 6328872 B1	18										USPAT
13	US 6322674 B1	34										USPAT

US-PAT-NO: 6328872

DOCUMENT-IDENTIFIER: US 6328872 B1

TITLE: Method and apparatus for plating and polishing a semiconductor substrate

---------- KWIC ----------

Brief Summary Text - BSTX (4):

A conventional process step in the manufacturing of integrated circuits and devices involves plating a metal layer on a semiconductor wafer surface using a plating apparatus. Typically, the wafer surface has been previously etched and contains many holes and/or trenches. One goal of wafer plating is to uniformly fill the holes and trenches with a conductive material. However, it is very difficult to uniformly fill the holes and trenches such that no voids exist. It is well known that the existence of the voids results in poor performance and defective devices. After such plating step, a polishing step is typically performed using a polishing apparatus to achieve a generally planar surface on the wafer .

Brief Summary Text - BSTX (5):

Plating the wafer surface with the conductive material over a seed metal layer has important and broad application in the semiconductor industry. Traditionally, aluminum and other metals are plated as one of many metal layers that make up a semiconductor chip. However, in recent times, there is great interest in copper deposition for interconnects on semiconductor chips, because, compared to aluminum, copper reduces electrical resistance and allows semiconductor chips to run faster with less heat generation, resulting in a significant gain in chip capacity and efficiency. Furthermore, copper is known to be a better conductor than aluminum.

Detailed Description Text - DETX (2):

The preferred embodiments of the present invention will now be described with reference to FIGS. 1-12. As noted above, conventional processing uses different equipment, at different times, to obtain conductive material within holes and trenches, or at other desired locations on the surface of a semiconductor wafer that contains many different semiconductor chips. Accordingly, the equipment cost needed to manufacture a high quality semiconductor integrated circuit device can be exorbitant.

Detailed Description Text - DETX (3):

The present invention contemplates different embodiments, which allow for the same apparatus, to be used to plate/deposit a conductive material onto the surface and into the contact, via holes, and trenches, as well as to polish the wafer surface. While the present invention can be used with any conductive material, it is especially suited for use with copper as the conductor, and for use in the fabrication of ULSI integrated circuits having submicron features with large aspect ratios. Furthermore, although a semiconductor wafer will be

(12) **United States Patent**
Talleh et al.

(10) **Patent No.: US 6,328,872 B1**
(45) **Date of Patent: Dec. 11, 2001**

(54) **METHOD AND APPARATUS FOR PLATING AND POLISHING A SEMICONDUCTOR SUBSTRATE**

(75) Inventors: Homayoun Talleh, San Jose; Cyprian Emeka Uzoh, Milpitas, both of CA (US)

(73) Assignee: Nutool, Inc., Milpitas, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/285,621

(22) Filed: Apr. 3, 1999

(51) Int. Cl.[7] C25D 17/00; C25D 5/34; C25D 5/52; C25B 9/00; C25B 11/00

(52) U.S. Cl. ..... 205/206; 205/219; 205/222; 204/212; 204/217; 204/224 R; 204/224 M; 204/252; 204/280

(58) Field of Search ..... 204/224 M, 224 R, 204/280, 271, 212-215, 217, 297 R, 252; 205/287, 222, 649, 206, 219, 220; 118/429

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,395,092	7/1968	Ribes .	
3,436,259	4/1969	Regh et al. .	
3,890,746	6/1975	Saegusa et al. .	
3,959,089	5/1976	Watts .	
4,153,523 *	5/1979	Koontz et al.	205/206 X
4,395,320 *	7/1983	Kasashima et al.	205/222 X
4,610,772	9/1986	Pahik .	

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

2008664	9/1971	(DE) .
4324330	3/1994	(DE) .
0903774 A2	3/1999	(EP) .
0960698 A2	12/1999	(EP) .
WO95/00295	1/1995	(WO) .

OTHER PUBLICATIONS

M. Rubinstein, "Tampongalvanisieren in der Praxis, Teil 1." *Galvanotechnik*, vol. 79, No. 10, 1988, pp. 3253–3270, (No month).

J.M. Steigerwald, R. Zirpoli, S.P. Murarka, D. Price and R.J. Gutman, "Pattern Geometry Effects in the Chemical-Mechanical Polishing of Inlaid Copper Structures", Oct. 1994, p. 2842–2848.

Alan C. West, Chih-Chang Cheng and Brett C. Baker, "Pulse Reverse Copper Electrodeposition in High Aspect Ratio Trenches and Vias", Sep. 1998, p. 3070–3073.

Robert C. Contolini, Anthony F. Bernhardt and Steven Mayer, "Electrochemical Planarization for Multilevel Metallization", Sep. 1994, p. 2503–2510.

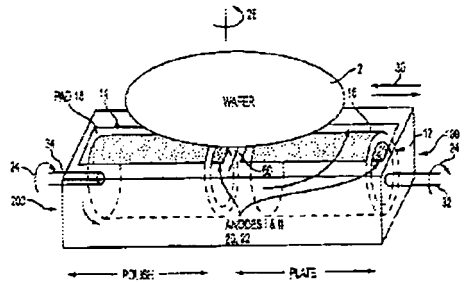
C. Madore, M. Matlosz and D. Landolt, "Blocking Inhibitors in Cathodic Leveling", I. Theoretical Analysis, Dec. 1996, p. 3927–3942.

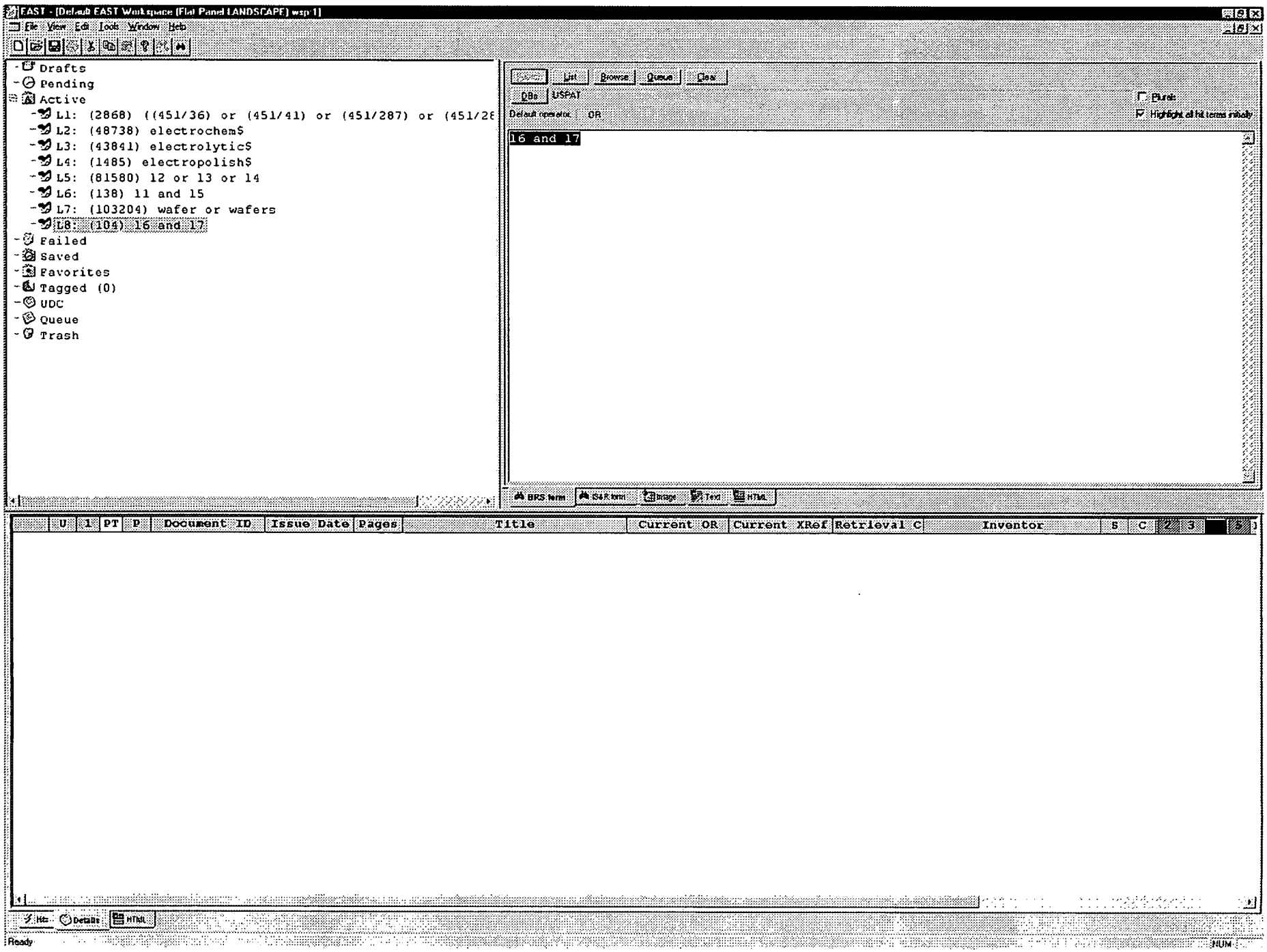
Primary Examiner—Donald R. Valentine
(74) *Attorney, Agent, or Firm*—Pillsbury Winthrop LLP

(57) **ABSTRACT**

The present invention provides a method and apparatus that plates/deposits a conductive material on a semiconductor substrate and then polishes the same substrate. This is achieved by providing multiple chambers in a single apparatus, where one chamber can be used for plating/depositing the conductive material and another chamber can be used for polishing the semiconductor substrate. The plating/depositing process can be performed using brush plating or electro chemical mechanical deposition and the polishing process can be performed using electropolishing or chemical mechanical polishing. The present invention further provides a method and apparatus for intermittently applying the conductive material to the semiconductor substrate and also intermittently polishing the substrate when such conductive material is not being applied to the substrate. Furthermore, the present invention provides a method and apparatus that plates/deposits and/or polishes a conductive material and improves the electrolyte mass transfer properties on a substrate using a novel anode assembly.

50 Claims, 10 Drawing Sheets




FAST - [Default FAST Workspace (Flat Panel LANDSCAPE) wsp 1]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (2868) ((451/36) or (451/41) or (451/287) or (451/28
L2: (48738) electrochem$
L3: (43841) electrolytic$
L4: (1485) electropolish$
L5: (81580) l2 or l3 or l4
L6: (138) l1 and l5
L7: (103204) wafer or wafers
L8: (104) l6 and l7
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash
Search
List
Browse
Queue
Clear
DBs
USPAT
Default operator:
OR
Plural
Highlight all hit terms initially
l6 and l7
BRS form
IS&R form
Image
Text
HTML
U
1
PT
P
Document ID
Issue Date
Pages
Title
Current OR
Current XRef
Retrieval C
Inventor
S
C
Hits
Details
HTML
Ready
NUM

EAST Browser - [8: (104) 6 and 7 | US 6379223 B1 | Tag: S | Doc: 16/104 (SORTED) | Format: KWIC

File Edit View Tools Window Help

	Document ID	Pages	1	2	3	4	5	6	S	C	P	Kind Codes	Sou
11	US 6428388 B1	36											USPAT
12	US 6413149 B1	37											USPAT
13	US 6402592 B1	11											USPAT
14	US 6390890 B1	36											USPAT
15	US 6379230 B1	29											USPAT
16	US 6379223 B1	13											USPAT
17	US 6375552 B1	15											USPAT

US-PAT-NO: 6379223

DOCUMENT-IDENTIFIER: US 6379223 B1

TITLE: Method and apparatus for electrochemical-mechanical planarization

---------- KWIC ---------

Abstract Text - ABTX (1):

A method for performing electrochemical-mechanical planarization (EMP) of a workpiece surface including a pattern of electrical conductors comprises supplying a chemical-mechanical polishing (CMP)-type apparatus having an abrasive or non-abrasive polishing pad with an oxidizer-free, electrolytically conductive, abrasive or non-abrasive fluid and applying a time-varying anodic potential to the workpiece surface for controllably dissolving the material, e.g., metal, of the electrical conductors while simultaneously applying mechanical polishing action to the surface. The method advantageously reduces or substantially eliminates undesirable dishing characteristic of conventional CMP planarization processing utilizing chemical oxidizer agent(s). Apparatus for performing EMP are also disclosed.

TITLE - TI (1):

Method and apparatus for electrochemical-mechanical planarization

Brief Summary Text - BSTX (2):

The present invention relates to a method and apparatus for electrochemically-assisted or -augmented mechanical planarization, i.e., electrochemical-mechanical planarization ("EMP"), which method and apparatus enjoy particular utility in the manufacture of semiconductor integrated circuit devices.

Brief Summary Text - BSTX (5):

Briefly, CMP processes utilized in semiconductor device manufacture involve mounting a thin flat workpiece, e.g., a semiconductor wafer substrate, on a carrier or polishing head, with the surface to be polished being exposed. The substrate surface is then urged against a wetted polishing surface, i.e., a rotating polishing pad, under controlled mechanical pressure, chemical, and temperature conditions. In addition, the carrier head may rotate to provide additional motion between the substrate and polishing pad surfaces. A polishing slurry containing a polishing agent, such as alumina (Al.sub.2 O.sub.3) or silica (SiO.sub.2) finely-dimensioned particles is used as the abrasive material. Additionally, the polishing slurry contains a number of chemicals, including pH adjusting and stabilizing agents, as well as chemical oxidizing agents for chemically removing (i.e., etching) various components of the surface being planarized. The combination of mechanical and chemical removal of surface material during the polishing process results in superior planarization of the polished surface, vis-a-vis other planarization techniques.

(12) **United States Patent**
Sun et al.

(10) **Patent No.: US 6,379,223 B1**
(45) **Date of Patent: Apr. 30, 2002**

(54) **METHOD AND APPARATUS FOR ELECTROCHEMICAL-MECHANICAL PLANARIZATION**

(75) Inventors: **Lizhong Sun**, Sunnyvale; **Stan D. Tsai**; **Fred C. Redeker**, both of Fremont, all of CA (US)

(73) Assignee: **Applied Materials, Inc.**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/450,937

(22) Filed: Nov. 29, 1999

(51) Int. Cl.[7] B24B 1/00

(52) U.S. Cl. 451/41; 451/287

(58) Field of Search 451/41, 63, 287, 451/288, 289, 397, 398

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,466,864	A	8/1984	Bacon, et al.
4,496,436	A	1/1985	Inoue
4,789,437	A	12/1988	Sing, et al.
4,839,005	A	6/1989	Katsumoto et al.
4,869,971	A	9/1989	Nee, et al.
4,956,056	A	9/1990	Zubatova et al.
5,032,238	A	7/1991	Ishimura et al.
5,039,381	A	8/1991	Mullarkey
5,096,550	A	3/1992	Mayer, et al.
5,114,548	A	5/1992	Rhoades
5,141,602	A	8/1992	Chen, et al.
5,217,586	A	6/1993	Datta, et al.
5,256,565	A	10/1993	Bernhardt, et al.
5,340,370	A	8/1994	Cadien et al.
5,522,965	A	6/1996	Chisholm et al.
5,637,031	A	6/1997	Chen
5,637,185	A *	6/1997	Murarka et al. 438/5
5,566,990	A	9/1997	Adams et al.
5,683,538	A	11/1997	O'Neill, et al.

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

JP	53-037543	4/1978	
WO	Wo 99/26758	6/1999	..... B24B/1/00
WO	WO 99/56527	10/1999	
WO	WO 00/26443	5/2000	
WO	WO 00/59682	10/2000	

OTHER PUBLICATIONS

C. Yu, et al., Appl. Phys. Let. "Dishing effects in a chemical mechanical polishing planarization process for advanced trench isolation", Sep. 14, 1992, pp. 1344–1346.

U.S. Patent Application Serial No. 09/450,658, filed on Nov. 29, 1999, 30 pages.

European Search Report from EP 00 31 0358, Dated Oct. 10, 2001.

09/569,883 Gandikota, et al.

09/289,074 Dordi, et al.

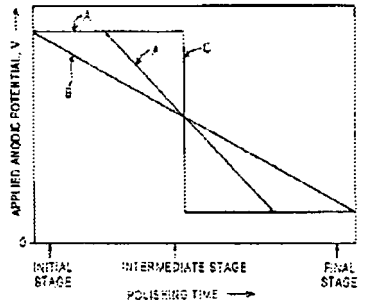
09/245,780 Dordi, et al.

Primary Examiner—Timothy V. Eley
Assistant Examiner—Dung Van Nguyen
(74) *Attorney, Agent, or Firm*—Moser, Patterson & Sheridan

(57) **ABSTRACT**

A method for performing electrochemical-mechanical planarization (EMP) of a workpiece surface including a pattern of electrical conductors comprises supplying a chemical-mechanical polishing (CMP)-type apparatus having an abrasive or non-abrasive polishing pad with an oxidizer-free, electrolytically conductive, abrasive or non-abrasive fluid and applying a time-varying anodic potential to the workpiece surface for controllably dissolving the material, e.g., metal, of the electrical conductors while simultaneously applying mechanical polishing action to the surface. The method advantageously reduces or substantially eliminates undesirable dishing characteristic of conventional CMP planarization processing utilizing chemical oxidizer agent(s). Apparatus for performing EMP are also disclosed.

5 Claims, 5 Drawing Sheets



FAST Browser - LB: (104) 6 and 7 | US 6368190 B1 | Tag: S | Doc: 21/104 (SORTED) | Format: KWIC

File Edit View Tools Window Help

	Document ID	Pages	1	2	3	4	5	U	S	C	P	Kind Codes	Sou
16	US 6379223 B1	13							☑				USPAT
17	US 6375552 B1	15							☑				USPAT
18	US 6375545 B1	18							☑				USPAT
19	US 6372111 B1	15							☑				USPAT
20	US 6368969 B1	7							☑				USPAT
21	US 6368190 B1	7							☑				USPAT
22	US 6361413 B1	8							☑				USPAT

US-PAT-NO: 6368190

DOCUMENT-IDENTIFIER: US 6368190 B1

TITLE: Electrochemical mechanical planarization apparatus and method

---------- KWIC ----------

Abstract Text - ABTX (1):

An apparatus for the electrochemical mechanical planarization of semiconductor wafers includes a rotatable platen and a polishing pad disposed on the platen. The polishing pad has top and bottom surfaces. A wafer carrier is disposed proximate to the platen for pressing a semiconductor wafer against the platen. At least one carrier electrode is disposed on the carrier and is adapted to electrically connect an electrically conducting surface of the semiconductor wafer to an electrolytic circuit including a potential source. A platen electrode is operatively connected to the platen. The platen electrode electrically connects an electrolytic solution disposed on the polishing pad to the potential source and to the electrode on the wafer carrier to complete the electrolytic circuit. The platen electrode has a substantially circular circumference for discharging electrons into the electrolytic solution. The platen electrode is substantially devoid of portions under the bottom surface of the polishing pad.

TITLE - TI (1):

Electrochemical mechanical planarization apparatus and method

Brief Summary Text - BSTX (7):

This invention relates generally to the field of semiconductor wafer fabrication, and more particularly to the field of electrochemical mechanical planarization (ECMP) of thin films used in semiconductor wafer fabrication.

Brief Summary Text - BSTX (9):

The production of integrated circuits begins with the creation of high quality semiconductor wafers . A semiconductor wafer typically includes a substrate, such as a silicon or gallium arsenide wafer, on which a plurality of transistors have been formed. Transistors are chemically and physically connected into a substrate by patterning regions in the substrate and layers on the substrate. The transistors are interconnected through the use of well known multilevel interconnects to form functional circuits. Typical multilevel interconnects are comprised of stacked thin films, with the interconnect layers consisting of one or more of the following: titanium (Ti), titanium nitrite (TiN), tantalum (Ta), aluminum-copper (Al--Cu), aluminum-silicon (Al--Si), copper (Cu), and tungsten (W).

Brief Summary Text - BSTX (10):

(12) **United States Patent**
Easter et al.

(10) **Patent No.: US 6,368,190 B1**
(45) **Date of Patent: Apr. 9, 2002**

(54) **ELECTROCHEMICAL MECHANICAL PLANARIZATION APPARATUS AND METHOD**

(75) Inventors: **William G. Easter; John A. Maze, III; Frank Micell, all of Orlando, FL (US)**

(73) Assignee: **Agere Systems Guardian Corp., Orlando, FL (US)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/491,836**

(22) Filed: **Jan. 26, 2000**

(51) Int. Cl.[7] **B24B 1/00**
(52) U.S. Cl. 451/41; 451/36; 451/287
(58) Field of Search 451/5, 36, 75, 451/41, 287, 288

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,575,706 A * 11/1996 Tsai et al. ..... 451/36 X
5,597,442 A * 1/1997 Chen et al. ..... 451/287 X
5,624,300 A * 4/1997 Kishii et al. 451/36
5,647,792 A * 7/1997 Katsuoka et al. ..... 451/287 X
5,827,114 A * 10/1998 Yam et al. 451/75
5,911,619 A 6/1999 Uzoh et al.

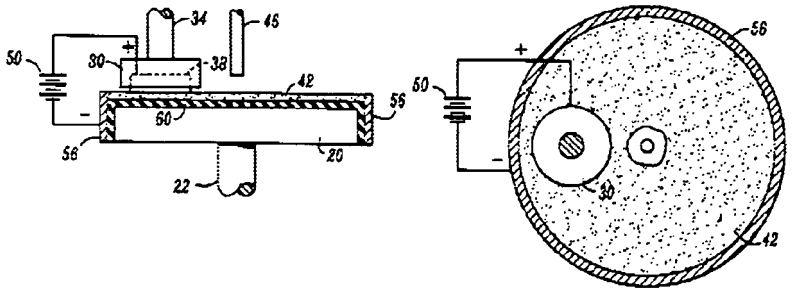
* cited by examiner

Primary Examiner—Joseph J. Hail, III
Assistant Examiner—Anthony Ojini

(57) **ABSTRACT**

An apparatus for the electrochemical mechanical planarization of semiconductor wafers includes a rotatable platen and a polishing pad disposed on the platen. The polishing pad has top and bottom surfaces. A wafer carrier is disposed proximate to the platen for pressing a semiconductor wafer against the platen. At least one carrier electrode is disposed on the carrier and is adapted to electrically connect an electrically conducting surface of the semiconductor wafer to an electrolytic circuit including a potential source. A platen electrode is operatively connected to the platen. The platen electrode electrically connects an electrolytic solution disposed on the polishing pad to the potential source and to the electrode on the wafer carrier to complete the electrolytic circuit. The platen electrode has a substantially circular circumference for discharging electrons into the electrolytic solution. The platen electrode is substantially devoid of portions under the bottom surface of the polishing pad.

12 Claims, 2 Drawing Sheets



EAST Browser - [8: (104) 6 and 7 | US 6242343 B1 | Tag: S | Doc: 43/104 (SORTED) | Format : KWIC]

File Edit View Tools Window Help

	Document ID	Pages	1	2	3	4	U	S	C	P	Kind Codes	Sou
38	US 6276987 B1	9										USPAT
39	US 6270395 B1	17										USPAT
40	US 6267644 B1	32										USPAT
41	US 6264536 B1	7										USPAT
42	US 6258231 B1	11										USPAT
43	US 6242343 B1	10										USPAT
44	US 6234877 B1	10										USPAT

US-PAT-NO: 6242343

DOCUMENT-IDENTIFIER: US 6242343 B1

TITLE: Process for fabricating semiconductor device and apparatus for fabricating semiconductor device

---------- KWIC ---------

Abstract Text - ABTX (1):

A process for fabricating a semiconductor device having a multilayer wiring, comprising steps of: forming a first wiring or electrode on a substrate; forming an insulating film which covers the first wiring or electrode; forming a contact hole to the first wiring or electrode through the insulating film; forming a wiring for contacting the first wiring or electrode inside the contact hole; and removing the protruded portion of the contact wiring and flattening the insulating film at the same time in an electrolytic solution by means of chemical mechanical polishing using the contact wiring as the anode. Also claimed is an apparatus for polishing the surface of a semiconductor device during its fabricating the device, comprising: means for performing chemicomechanical polishing; and means for supplying electric current to the electrode of the semiconductor device.

Brief Summary Text - BSTX (15):

According to an aspect of the present invention, there is provided a process for fabricating a semiconductor device having a multilayer wiring structure, characterized by comprising the steps of: forming a first wiring or electrode on a substrate; forming an insulating film which covers the first wiring or electrode; forming a contact hole to the first wiring or electrode through the insulating film; forming a wiring for contacting the first wiring or electrode inside the contact hole; and removing the protruded portion of the contact wiring and flattening the insulating film at the same time in an electrolytic solution by means of chemical mechanical polishing using the contact wiring as the anode.

Brief Summary Text - BSTX (16):

According to another aspect of the present invention, there is provided a process for polishing the surface of a semiconductor device during its fabrication, characterized by comprising performing electrolytic polishing using the electrode of the semiconductor device as the anode while performing chemical mechanical polishing at the same time.

Brief Summary Text - BSTX (19):

According to the present invention disclosed in the specification, an electrolytic solution having an electric resistance in a range of from 10.sup.-3 to 10.sup.10 (.OMEGA..multidot.cm).sup.-1 is used.

Detailed Description Text - DETX (19):

(12) **United States Patent**
Yamazaki et al.

(10) **Patent No.: US 6,242,343 B1**
(45) **Date of Patent: *Jun. 5, 2001**

(54) **PROCESS FOR FABRICATING SEMICONDUCTOR DEVICE AND APPARATUS FOR FABRICATING SEMICONDUCTOR DEVICE**

(75) Inventors: **Shunpei Yamazaki**, Tokyo; **Satoshi Teramoto**, Kanagawa, both of (JP)

(73) Assignee: **Semiconductor Energy Laboratory Co., Ltd.**, Kanagawa-Ken (JP)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 08/794,879

(22) Filed: **Feb. 5, 1997**

(30) **Foreign Application Priority Data**

Feb. 5, 1996 (JP) 8-042149

(51) Int. Cl.[7] H01L 21/4763

(52) U.S. Cl. 438/633; 438/691; 438/692; 451/41

(58) Field of Search 438/633, 625, 438/692, 691, 690, 720; 451/36, 41, 285

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,391,258	*	2/1995	Brancaleoni et al.	156/636
5,562,529	*	10/1996	Kishii et al.	451/36
5,567,300	*	10/1996	Datta et al.	205/652
5,575,706	*	11/1996	Tsai et al.	451/41
5,616,934	*	4/1997	Donahoe et al.	257/67
5,658,806	*	8/1997	Lin et al.	438/159
5,807,163	*	9/1998	Ueda et al.	451/41

FOREIGN PATENT DOCUMENTS

7-136848 5/1995 (JP).

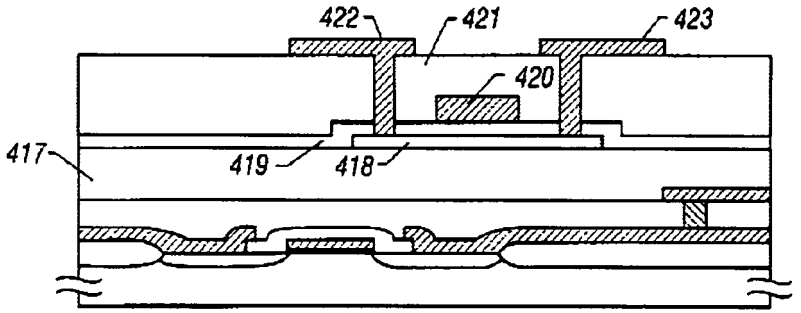
* cited by examiner

Primary Examiner—Caridad Everhart
(74) *Attorney, Agent, or Firm*—Fish & Richardson

(57) **ABSTRACT**

A process for fabricating a semiconductor device having a multilayer wiring, comprising steps of forming a first wiring or electrode on a substrate; forming an insulating film which covers the first wiring or electrode; forming a contact hole to the first wiring or electrode through the insulating film; forming a wiring for contacting the first wiring or electrode inside the contact hole; and removing the protruded portion of the contact wiring and flattening the insulating film at the same time in an electrolytic solution by means of chemical mechanical polishing using the contact wiring as the anode. Also claimed is an apparatus for polishing the surface of a semiconductor device during its fabricating the device, comprising: means for performing chemicomechanical polishing; and means for supplying electric current to the electrode of the semiconductor device.

29 Claims, 3 Drawing Sheets



EAST Browser - L8: [104] 6 and 7 | US 6191040 B1 | Tag: S | Doc: 49/104 (SORTED) | Format: KWIC

File Edit View Tools Window Help

	Document ID	Pages	1	2	3	4	U	S	C	P	Kind Codes	Sou
44	US 6234877 B1	10						☑				USPAT
45	US 6234870 B1	19						☑				USPAT
46	US 6231427 B1	15						☑				USPAT
47	US 6217416 B1	9						☑				USPAT
48	US 6204169 B1	8						☑				USPAT
49	US 6191040 B1	11						☑				USPAT
50	US 6171467 B1	9						☑				USPAT

US-PAT-NO: 6191040

DOCUMENT-IDENTIFIER: US 6191040 B1

TITLE: Wafer surface treatment methods and systems using electrocapillarity

---------- KWIC ---------

TITLE - TI (1):

Wafer surface treatment methods and systems using electrocapillarity

Brief Summary Text - BSTX (2):

The present invention relates to methods and systems for use in integrated circuit fabrication. More particularly, the present invention relates to the use of electrocapillarity in the treatment of wafer surfaces, e.g., planarization, coating, etc.

Brief Summary Text - BSTX (4):

In semiconductor wafer processing, various surface treatment steps are commonly performed. For example, such surface treatment may include application of a coating on the wafer surface or planarizing an exposed wafer surface prior to subsequent processing steps.

Brief Summary Text - BSTX (5):

Planarization, such as chemical-mechanical planarization (CMP), is typically performed to achieve a planar surface over a wafer, sometimes referred to as "global planarity." Typically, the planarization process involves a rotating wafer holder that holds a wafer. A slurry is applied to a rotating table or platen which has a polishing pad thereon. The polishing pad is applied to the wafer at a certain pressure to perform the planarization. In some planarization processes, the wafer holder may not rotate, the table or platen may not rotate and/or the platen may be moved in a linear motion as opposed to rotating. There are numerous types of planarization units available which perform the process in different manners.

Brief Summary Text - BSTX (6):

In many circumstances, even after planarization has been performed, surface nonuniformities of the wafer are present. For example, because of different rotational speeds of the process at the center of the wafer as opposed to the edge of the wafer and different rotational speeds of the rotating table at the center and at the rotating table's periphery, the rate of removal tends to be different across the wafer surface. For example, the removal rate at the edge of the wafer may be higher than at the center of the wafer. Further, for example, the slurry may not be adequately transported to the entire contact area between the wafer and the pad such that further rate of removal differences are created. Slurry transport to the center of the wafer may also

(12) **United States Patent**
Glass

(10) **Patent No.: US 6,191,040 B1**
(45) **Date of Patent: Feb. 20, 2001**

(54) **WAFER SURFACE TREATMENT METHODS AND SYSTEMS USING ELECTROCAPILLARITY**

(75) Inventor: **Thomas R. Glass**, Idaho City, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

(21) Appl. No.: 09/453,484

(22) Filed: Dec. 17, 1999

Related U.S. Application Data

(63) Continuation of application No. 08/915,157, filed on Aug. 20, 1997, now Pat. No. 6,010,964.

(51) Int. Cl.[7] H01L 21/00

(52) U.S. Cl. 438/692; 156/345; 118/232; 216/38; 451/36; 451/285; 438/693; 438/697

(58) Field of Search ..... 438/691, 692, 438/693, 697, 699, 747, 748, 782; 118/218, 232; 216/38, 88, 89; 451/36, 41, 285; 156/345 LP

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,193,225	3/1980	Gill, Jr. et al.	51/124 R
4,811,522	3/1989	Gill, Jr.	51/131.1
5,421,769	6/1995	Kurtin	434/109
5,533,924	7/1995	Stroupe et al.	451/285
5,575,705 *	11/1996	Tsai et al.	438/693
5,637,185	6/1997	Murarka et al.	438/693 X
6,010,964	1/2000	Glass .	

OTHER PUBLICATIONS

Esmail et al., "Air Entrainment and Dynamic Contact Angles in Hydrodynamics of Liquid Coating," *Canadian J. Chem. Engineer.*, 68:197–203 (1990).

Rillaerts et al., "The Dynamic Contact Angle," *Chem. Engineer. Sci.*, 35:883–887 (1980).

Steigerwald et al., "Electrochemical Chemical Potential Measurements during the Chemical–Mechanical Polishing of Copper Thin Films," *J. Electrochem. Soc.*, 142:2379–2385 (1995).

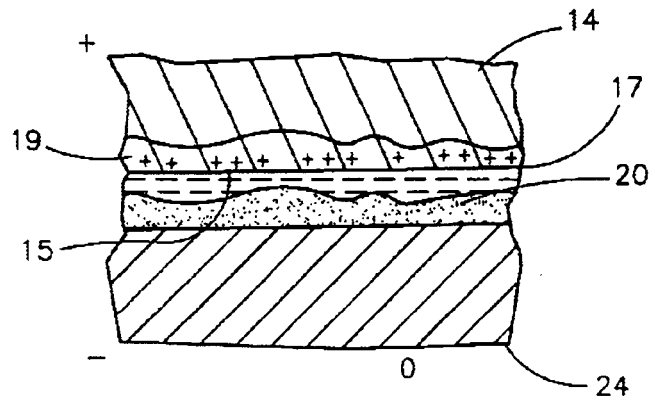
* cited by examiner

Primary Examiner—William Powell
(74) *Attorney, Agent, or Firm*—Mueting, Raasch & Gebhardt, P.A.

(57) **ABSTRACT**

A surface treatment method for use in integrated circuit fabrication includes providing a substrate assembly having a surface. A liquid is provided adjacent the surface resulting in an interface therebetween. An electrical potential difference is applied across the interface and the surface is treated as the electrical potential difference is applied across the interface. The liquid may be a planarization liquid when the treatment of the surface includes planarizing a substrate assembly or the liquid may be a coating material when the treatment of the surface includes applying a coating material on the surface.

28 Claims, 4 Drawing Sheets



See fig 2
wafer positive

EAST Browser - LB: [104] 6 and 7 | US 6113464 A | Tag: S | Doc: 54/104 (SORTED) | Format: KWIC

File Edit View Tools Window Help

	Document ID	Pages	1	2	3	4	5	6	S	C	P	Kind Codes	Sou
49	US 6191040 B1	11											USPAT
50	US 6171467 B1	9											USPAT
51	US 6149506 A	93											USPAT
52	US 6120354 A	10											USPAT
53	US 6120352 A	38											USPAT
54	US 6113464 A	17											USPAT
55	US 6110011 A	10											USPAT

US-PAT-NO: 6113464

DOCUMENT-IDENTIFIER: US 6113464 A

TITLE: Method for mirror surface grinding and grinding wheel therefore

---------- KWIC ---------

Abstract Text - ABTX (1):

An apparatus and a method for mirror surface grinding which enables high quality, stable ELID grinding; and a grinding wheel for electrolytic dressing. The apparatus comprises a grinding wheel 3 having a contact surface 2 for contacting a workpiece 1, an electrode 4 facing the surface 2, nozzles 5 for supplying conductive fluid between the grinding wheel 3

Abstract Text - ABTX (2):

and the electrode 4, and a power source 6 and feeder 7 for applying a voltage between the grinding wheel and the electrode 4. The bond material, which is selected from among iron, ferrous metal, cobalt, nickel and combinations of two or more thereof, along with grains and sintering aid are molded together and sintered to obtain the conductive grinding wheel. Next, a conductive water-soluble grinding fluid containing an alkanolamine and anions is supplied between the grinding wheel and the electrode, and a pulse wave voltage is applied between the grinding wheel and the electrode to dress the grinding wheel electrolytically during grinding.

Brief Summary Text - BSTX (2):

The present invention relates to an apparatus and a method for mirror surface grinding and a grinding wheel for grinding a mirror surface. More particularly, the present invention relates to an apparatus and a method for electrolytically dressing a conductive grinding wheel and for grinding a workpiece to a mirror surface finish with the grinding wheel. The present invention also relates to a grinding wheel exhibiting mechano-chemical action for electrolytic dressing.

Brief Summary Text - BSTX (4):

In the 1960's, Norton Company of the USA achieved electrolytic dressing of grinding wheels by reversing the potential between the grinding wheel and the workpiece in conventional electrolytic grinding. In 1983, The Mechanical Engineering Laboratory of the Japanese Agency of Industry and Science Technology reported in Japanese Patent Publication No. 63-9945 that stable cutting could be obtained by (1) applying a direct current between a bronze bonded grinding wheel and an electrode, and (2) supplying a grinding fluid as an electrolyte between the grinding wheel and the electrode. However, since the above electrolytic dressing methods use bronze metal bonded wheels, a direct current power supply, and a conventional grinding fluid as an electrolyte, they can be used only for rough grinding. A high quality finish such as a mirror surface can not be obtained by such grinding methods.

United States Patent [19]

Ohmori et al.

[11] **Patent Number: 6,113,464**

[45] **Date of Patent: Sep. 5, 2000**

[54] **METHOD FOR MIRROR SURFACE GRINDING AND GRINDING WHEEL THEREFORE**

[75] Inventors: **Hitoshi Ohmori**; **Katsuhiko Katkomi**, both of Tokyo, Japan

[73] Assignee: **Rikagaku Kenkyusho**, Saitama-ken, Japan

[21] Appl. No.: 08/742,447

[22] Filed: Nov. 1, 1996

Related U.S. Application Data

[60] Continuation of application No. 08/380,615, Jan. 30, 1995, abandoned, which is a division of application No. 08/079,379, Jun. 21, 1993, abandoned.

[30] **Foreign Application Priority Data**

Jun. 19, 1992 [JP] Japan 159882
Mar. 4, 1993 [JP] Japan 44143

[51] Int. Cl.[7] B24B 1/00

[52] U.S. Cl. 451/41; 451/56

[58] Field of Search 451/63, 41, 56, 451/541, 550; 205/662, 663

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,905,162	9/1975	Lawrence et al.	451/63 X
4,064,662	12/1977	Langen	451/63 X
4,236,985	12/1980	Grodzinsky et al.	
4,448,656	5/1984	Kuromatsu	205/663 X
4,512,859	4/1985	Inoue	205/662
4,588,473	5/1986	Hitatomi et al.	451/63 X
4,849,595	7/1989	Kuromatsu	
4,977,710	12/1990	Une	
5,157,876	10/1992	Medellin	451/63 X
5,313,742	5/1994	Concoras, Jr. et al.	451/541

FOREIGN PATENT DOCUMENTS

1251037	11/1986	Japan	451/63
722803	3/1992	U.S.S.R.	

OTHER PUBLICATIONS

Japanese Patent Abstract Publication No. 1-188266, date Jul. 27, 1989.
Japanese Patent Abstract Publication No. 02-095574, date Apr. 6, 1990.
Japanese Patent Abstract Publication No. 02-232162, date Sep. 14, 1990.
Japanese Patent Abstract Publication No. 02-232163, date Sep. 14, 1990.
Japanese Patent Abstract Publication No. 04-25365, date Jan. 29, 1992.
Japanese Patent Abstract Publication No. 04-115867, date Apr. 16, 1992.
Japanese Patent Abstract Publication No. 04-275874, date Oct. 1, 1992.
Japanese Patent Abstract Publication No. 54-84686, date May 7, 1979.

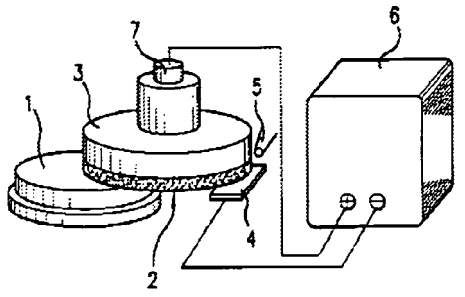
(List continued on next page.)

Primary Examiner—Timothy V. Eley
Attorney, Agent, or Firm—Griffin & Szipl, P.C.

[57] **ABSTRACT**

An apparatus and a method for mirror surface grinding which enables high quality, stable ELID grinding, and a grinding wheel for electrolytic dressing. The apparatus comprises a grinding wheel 3 having a contact surface 2 for contacting a workpiece 1, an electrode 4 facing the surface 2, nozzles 5 for supplying conductive fluid between the grinding wheel 3 and the electrode 4, and a power source 6 and feeder 7 for applying a voltage between the grinding wheel and the electrode 4. The bond material, which is selected from among iron, ferrous metal, cobalt, nickel and combinations of two or more thereof, along with grains and sintering aid are molded together and sintered to obtain the conductive grinding wheel. Next, a conductive water-soluble grinding fluid containing an alkanolamine and anions is supplied between the grinding wheel and the electrode, and a pulse wave voltage is applied between the grinding wheel and the electrode to dress the grinding wheel electrolytically during grinding.

13 Claims, 7 Drawing Sheets



EAST Browser - L8: (104) 6 and 7 | US 6090239 A | Tag: S | Doc: 58/104 (SORTED) | Format: KWIC

File Edit View Tools Window Help

	Document ID	Pages	1	2	3	4	5	6	S	C	P	Kind Codes	Sou
53	US 6120352 A	38							☑				USPAT
54	US 6113464 A	17							☑				USPAT
55	US 6110011 A	10							☑				USPAT
56	US 6102777 A	72							☑				USPAT
57	US 6095899 A	14							☑				USPAT
58	US 6090239 A	9							☑				USPAT
59	US 6080050 A	17							☑				USPAT

US-PAT-NO: 6090239

DOCUMENT-IDENTIFIER: US 6090239 A

TITLE: Method of single step damascene process for deposition and global planarization

---------- KWIC ---------

Abstract Text - ABTX (1):

A modified chemical-mechanical polishing apparatus is described. The apparatus includes: (i) a polishing pad 104 providing a surface against which a surface of an integrated circuit substrate 116 is polished; (ii) an anode 103 on which the polishing pad is secured, the anode including an electrolyzable conductive material; and (iii) a voltage source 106 electrically connecting the anode to the integrated circuit substrate in such a way that when a voltage is applied from the voltage source in the presence of slurry 114 admixed with an electrolyte composition on the polishing pad, an electrolytic cell results in which the conductive material deposits on the surface of the integrated circuit substrate. A process of depositing a conductive material on and polishing a surface of an integrated circuit substrate simultaneously is also described.

Brief Summary Text - BSTX (6):

Next, a metallization layer 20 is blanket deposited on partially the fabricated IC substrate surface, as shown in FIG. 1B, filling trench 16 and via hole 18 of FIG. 1A to form a metal line 16' and a via plug 18', respectively. The IC substrate surface then undergoes chemical-mechanical polishing (CMP) to remove the excess metallization layer 20 deposited above dielectric layer 14 and above metal line 16'. CMP typically involves mounting an IC substrate, e.g., a semiconductor wafer, faced down on a substrate holder and rotating the substrate surface against a polishing pad mounted on a platen, which is in turn rotating or is in orbital state. A slurry containing a chemical that chemically interacts with the facing substrate layer and an abrasive that physically removes that layer is flowed between the substrate surface and the polishing pad or on the pad near the substrate surface.

Brief Summary Text - BSTX (11):

To achieve the foregoing, the present invention provides a modified chemical-mechanical polishing apparatus. The apparatus includes: (i) a polishing pad for providing a surface against which a surface of an integrated circuit substrate is polished during polishing, (ii) an anode on which the polishing pad is secured, the anode including an electrolyzable conductive material; and (iii) a voltage source including a first electrical connection and a second electrical connection, the first electrical connection being connected to the anode and the second electrical connection being configured for connection to the integrated circuit substrate undergoing polishing such that when a voltage is applied from the voltage source in the presence of slurry admixed with an electrolyte composition on the polishing pad, an electrolytic cell results in which the conductive material deposits on the surface of the integrated circuit substrate.

United States Patent [19]

Liu et al.

[11] **Patent Number: 6,090,239**

[45] **Date of Patent: Jul. 18, 2000**

[54] **METHOD OF SINGLE STEP DAMASCENE PROCESS FOR DEPOSITION AND GLOBAL PLANARIZATION**

[75] Inventors: **Yauh-Ching Liu**, Sunnyvale; **Dung-Ching Perng**, San Jose, both of Calif.

[73] Assignee: **LSI Logic Corporation**, Milpitas, Calif.

[21] Appl. No.: 09/365,440

[22] Filed: Aug. 2, 1999

Related U.S. Application Data

[62] Division of application No. 08/627,507, Feb. 20, 1996.

[51] Int. Cl.[7] C23F 1/02

[52] U.S. Cl. 156/345; 451/67; 451/73; 451/287; 451/290

[58] Field of Search 156/345; 451/67, 451/287, 290, 461, 73; 204/227

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,723,387	3/1998	Chen	438/692
5,807,165	9/1998	Uzoh et al.	451/41
5,911,619	6/1999	Uzoh et al.	451/5

OTHER PUBLICATIONS

Morand et al., "Copper Integration in Self Aligned Dual Damascene Architecture", 1997, Symposium on VLSI Technology Digest of Technical Papers, pp. 31–32.

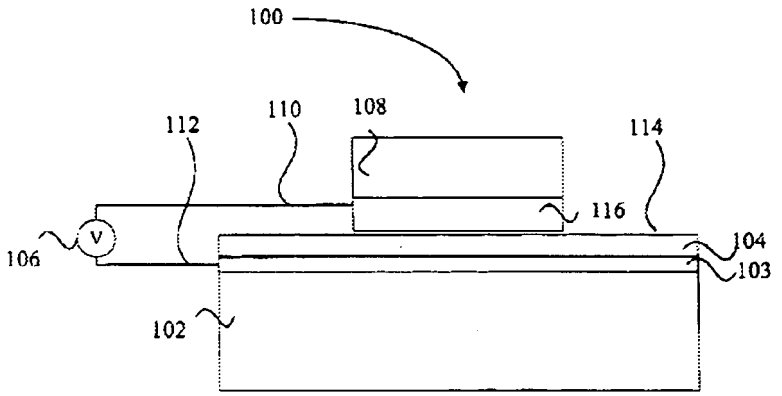
Tsuchiya et al., "Ultra-Low Resistance Direct Contact Cu Via Technology Using In-Situ Chemical Vapor Cleaning", 1997, Symposium on VLSI Technology Digest of Technical Papers, pp. 59–60.

Primary Examiner—Benjamin L. Utech
Assistant Examiner—Donald L. Champagne
Attorney, Agent, or Firm—Beyer & Weaver, LLP

[57] **ABSTRACT**

A modified chemical-mechanical polishing apparatus is described. The apparatus includes: (i) a polishing pad 104 providing a surface against which a surface of an integrated circuit substrate 116 is polished; (ii) an anode 103 on which the polishing pad is secured, the anode including an electrolyzable conductive material; and (iii) a voltage source 106 electrically connecting the anode to the integrated circuit substrate in such a way that when a voltage is applied from the voltage source in the presence of slurry 114 admixed with an electrolyte composition on the polishing pad, an electrolytic cell results in which the conductive material deposits on the surface of the integrated circuit substrate. A process of depositing a conductive material on and polishing a surface of an integrated circuit substrate simultaneously is also described.

8 Claims, 4 Drawing Sheets



EAST Browser - LB: (104) 6 and 7 | US 6066030 A | Tag: S | Doc: 60/104 (SORTED) | Format: KWIC

File Edit View Tools Window Help

	Document ID	Pages	1	2	3	4	5	6	S	C	P	Kind Codes	Sou
55	US 6110011 A	10											USPAT
56	US 6102777 A	72											USPAT
57	US 6095899 A	14											USPAT
58	US 6090239 A	9											USPAT
59	US 6080050 A	17											USPAT
60	US 6066030 A	8											USPAT
61	US 6022400 A	13											USPAT

US-PAT-NO: 6066030

DOCUMENT-IDENTIFIER: US 6066030 A

TITLE: Electroetch and chemical mechanical polishing equipment

---------- KWIC ----------

Brief Summary Text - BSTX (6):

Comparatively high cost associated with damascene chip wiring methods and the apparatus utilized in such methods is typically due mostly to lower throughput. Throughput associated with such methods can range from about 3 wafers per hour for levels with relatively wide wire lines, to as high as 8 wafers per hour for thinner metal lines. Typically, for full damascene BEOL, the limited throughput and chemical mechanical polishing typically require additional polishing tools and a subsequent increase in space for the fabrication line to result in a desired level of throughput.

Detailed Description Text - DETX (16):

Also, the cathode may be removable. Whether removable or not, the cathode may be located about 2 to 3 mm from the walls of the polishing head. An easily detachable cathode may be fabricated from stainless steel or titanium or other suitable materials. As seen in FIG. 2, the cathode may include inlets 5b and 5c for at least one etching or polishing solution. The cathode may also include channel 5d for outlet or discharge of the etching or electropolishing solution on the workpiece 3.

Detailed Description Text - DETX (26):

Further arranged adjacent to the polishing head may be at least one second sensor 27 to detect a polishing end point. For example, the end point detector could be an electrochemical sensor calibrated to detect the transition of one type of material to another. For example, the at least one sensor could include a pH sensor. Such a sensor could detect changing conditions as a change occurs from one chemical reaction to another.

Detailed Description Text - DETX (27):

Typically, sensor 25 and 27 operate in a collaborative manner. For instance, sensor 25 may initially quickly measure the thickness and profile of material such as metal deposited on the workpiece. From this information, the sensor may select the optimum recipe of electropolishing and/or CMP processes required.

Detailed Description Text - DETX (28):

After electropolishing and/or CMP processes are initiated, toward a later part of the CMP process, sensor 25 may activate sensor 27. With both sensors activated, they may both work in a collaborative manner. For example, in the polishing of copper films with a tantalum barrier layer in a damascene type

United States Patent [19]

Uzoh

[11] Patent Number: 6,066,030

[45] Date of Patent: May 23, 2000

[54] ELECTROETCH AND CHEMICAL MECHANICAL POLISHING EQUIPMENT

[75] Inventor: Cyprian E. Uzoh, Hopewell Junction, N.Y.

[73] Assignee: International Business Machines Corporation, Armonk, N.Y.

[21] Appl. No.: 09/262,691

[22] Filed: Mar. 4, 1999

[51] Int. Cl.[7] B24B 1/00; B24B 29/00

[52] U.S. Cl. 451/41; 451/287

[58] Field of Search 451/41, 63, 287, 451/288, 289, 397, 398, 54; 156/345, 636.1

[56] References Cited

U.S. PATENT DOCUMENTS

4,435,247	3/1984	Basi et al. .	
4,466,218	8/1984	Ottman et al. .	
4,527,355	7/1985	Day .	
4,549,374	10/1985	Besi et al. .	
4,728,552	3/1988	Jensen, Jr. .	
4,750,915	6/1988	Tomita et al. .	
4,839,005	6/1989	Kazumoto et al. .	
4,841,680	6/1989	Hoffstein et al. .	
4,842,678	6/1989	Nara et al. .	
4,876,220	10/1989	Kaanzabe .	
4,910,155	3/1990	Cote et al. .	
4,934,102	6/1990	Leach et al. .	
4,944,119	7/1990	Gill, Jr. et al. .	
4,980,036	12/1990	Saito et al. .	
5,020,283	6/1991	Tuttle .	
5,036,630	8/1991	Kaanta et al. .	
5,076,024	12/1991	Akagawa et al. .	
5,081,421	1/1992	Miller et al. .	
5,108,561	4/1992	Kurometsu	
5,177,908	1/1993	Tuttle .	
5,194,126	3/1993	Packella .	
5,431,766	7/1995	Propst et al.	156/345
5,575,706	11/1996	Tsai et al. .	
5,643,406	7/1997	Shimomura et al.	156/636.1
5,660,579	8/1997	Nakayama et al. .	
5,807,165	9/1998	Uzoh .	

FOREIGN PATENT DOCUMENTS

284 343 B1 11/1990 European Pat. Off. .

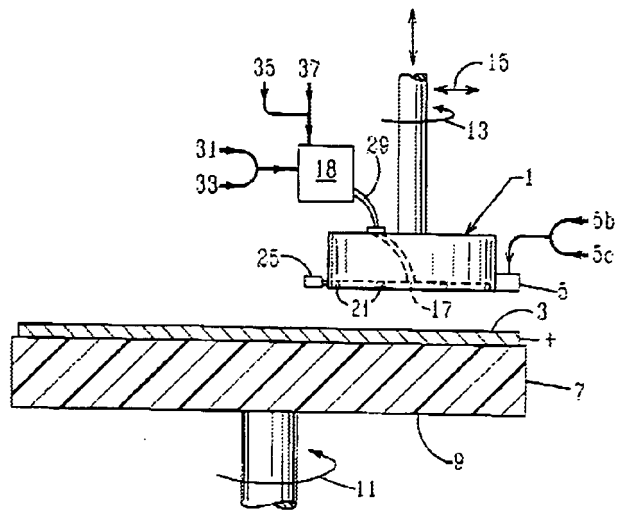
Primary Examiner—Rodney A. Butler

Attorney, Agent, or Firm—Pollock, Vande Sande & Amernick

[57] ABSTRACT

An apparatus for removing material from a substrate including a single platform comprising elements for performing electroetching and chemical mechanical polishing. A polishing head engages a surface of the substrate to polish the substrate. A cathode for electroetching material from the substrate. A substrate support supports a substrate to be treated. At least one slurry introduction port introduces polishing slurry between the polishing head and the substrate. A power supply supplies power to the anode and the cathode.

47 Claims, 2 Drawing Sheets



4/2003

solely electropolishing
never searched or crossed in 205

FAST Browser - LR: (104) 6 and 7 | US 6402592 B1 | Tag: S | Doc: 13/104 (SORTED) | Format: KWIC

File Edit View Tools Window Help

	Document ID	Pages	1	2	3	4	5	6	S	C	P	Kind Codes	Sou
8	US 6447371 B2	9							☑				USPAT
9	US 6435948 B1	57							☑				USPAT
10	US 6435947 B2	10							☑				USPAT
11	US 6428388 B1	36							☑				USPAT
12	US 6413149 B1	37							☑				USPAT
13	US 6402592 B1	11							☑				USPAT
14	US 6390890 B1	36							☑				USPAT

US-PAT-NO: 6402592

DOCUMENT-IDENTIFIER: US 6402592 B1

TITLE: Electrochemical methods for polishing copper films on semiconductor substrates

---------- KWIC ---------

Abstract Text - ABTX (1):

Methods for electrochemically polishing copper films on semiconductor substrates use an alkaline solution with a pH in the range of about 8.0 to 10.5. A constant current density of from 5 to 100 amperes per square foot is applied to an electrochemical cell formed by an electrode, the alkaline solution and the copper film. Copper is removed at a rate of from 500 to 10,000 angstroms per minute. The end point for the electro-polishing is detected by a sudden change in applied voltage. The alkaline polishing solution may also contain copper ions so that when the current direction is reversed, copper is deposited onto the copper film. Furthermore, this copper deposition will occur selectively on the exposed copper surface but not on the exposed barrier layer surface. Hence, the method can compensate for dishing and erosion by re-depositing copper in regions after too much copper was removed from those regions.

TITLE - TI (1):

Electrochemical methods for polishing copper films on semiconductor substrates

Brief Summary Text - BSTX (3):

This invention relates to the field of electrochemical deposition and removal of copper, and, more particularly, to electrochemically polishing copper films.

Brief Summary Text - BSTX (5):

In the manufacture of devices on semiconductor substrates, such as semiconductor wafers, multiple levels of conductive layers are applied to the substrate. In order to fabricate features, circuits, vias and devices on the substrate, various techniques are used to deposit and etch materials on the substrate. Deposition techniques include processes such as physical vapor deposition (PVD), chemical vapor deposition (CVD), and immersion of the substrate into an electrolyte solution. This last technique may be used for either electroless deposition or electroplating.

Brief Summary Text - BSTX (6):

Similarly, a number of techniques are known for removing a material from a wafer. These techniques include wet chemical etching, reactive ion etching (RIE), plasma etching, chemical mechanical polishing (CMP), and immersion of

(12) **United States Patent**
Zhu et al.

(10) **Patent No.: US 6,402,592 B1**
(45) **Date of Patent: Jun. 11, 2002**

(54) **ELECTROCHEMICAL METHODS FOR POLISHING COPPER FILMS ON SEMICONDUCTOR SUBSTRATES**

(75) Inventors: **Mei Zhu**, San Jose; **Igor Ivanov**, Measanton; **Chiu H. Ting**, Saratoga, all of CA (US)

(73) Assignee: **Stoag Cutek Systems, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/761,327

(22) Filed: Jan. 17, 2001

(51) Int. Cl.[7] B24B 1/00

(52) U.S. Cl. 451/36; 451/41; 451/907; 451/908

(58) Field of Search 451/36, 41, 905, 451/907, 908. 909

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,840,629	A	11/1998	Carpio
5,997,712	A	12/1999	Ting et al
6,017,437	A	1/2000	Ting et al.
6,153,043	A *	11/2000	Edelstein et al.

OTHER PUBLICATIONS

M. Bohr, "Interconnect Sealing—The Real Limiter to High Performance ULSI" *IEDM Technical Digest*, p. 241 (1995).
P. Pai and C. Ting, "Copper as the Future Interconnection Material," Proceedings of VMIC Conference (Jun. 12–13, 1989.) pp. 258–264.
S Venkatesan, et al., "High Performance 1.8V, 0.20 μm CMOS Technology with Copper Metallization," *IDEM Technical Digest*, pp. 31.2.1–31.3.4.
R. Contolini, et al., "Electrochemical Planarization for Multilevel Metallization," *J. Electrochem Soc.*, V. 141, No. 9, p. 2503 (1994).
S. Lopatin, et al., "Characterization of Electrodissolving Copper in Aqueous Acid Solution for Sub-Quarter Micron Interconnect Formation in Low k Materials" Extended Abstract No. 741, 196th Meeting of Electrochemical Soc., (1999).
E. Zielinski, et al., "Damascene Integration of Copper and Ultra-Low-k Xerogel for High Performance Interconnects."
R. Powell, et al., "Raising the IC Speed Limit by the Use of Copper Interconnects." (2000).
W. Dresher, "Speeding—up Your Computer in the 21st Century Using Copper ICs" (2000).
P. Singer, "Tantalum, Copper and Damascene: The Future of Interconnects" *Semiconductor International* (Jun. 1998).
A. Wolfe, "Copper upends the Semiconductor Design Landscape" EE Times.com (May 1998).

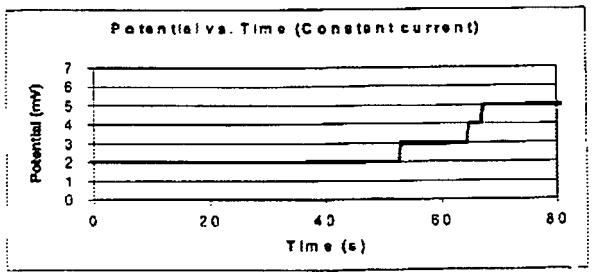
* cited by examiner

Primary Examiner—Joseph J. Hail, III
Assistant Examiner—Willie Berry, Jr.
(74) *Attorney, Agent, or Firm*—Connolly Bove Lodge & Hutz LLP

(57) **ABSTRACT**

Methods for electrochemically polishing copper films on semiconductor substrates use an alkaline solution with a pH in the range of about 8.0 to 10.5. A constant current density of from 5 to 100 amperes per square foot is applied to an electrochemical cell formed by an electrode, the alkaline solution and the copper film. Copper is removed at a rate of from 500 to 10,000 angstroms per minute. The end point for the electro-polishing is detected by a sudden change in applied voltage. The alkaline polishing solution may also contain copper ions so that when the current direction is reversed, copper is deposited onto the copper film. Furthermore, this copper deposition will occur selectively on the exposed copper surface but not on the exposed barrier layer surface. Hence, the method can compensate for dishing and erosion by re-depositing copper in regions after too much copper was removed from those regions.

39 Claims, 6 Drawing Sheets



EAST Browser - L8: (104) 6 and 7 | US 6402592 B1 | Tag: S | Doc: 13/104 (SORTED) | Format: KWIC

File Edit View Tools Window Help

	Document ID	Pages	1	2	3	4	5	U	S	C	P	Kind Codes	Sou
8	US 6447371 B2	9							☑				USPAT
9	US 6435948 B1	57							☑				USPAT
10	US 6435947 B2	10							☑				USPAT
11	US 6428388 B1	36							☑				USPAT
12	US 6413149 B1	37							☑				USPAT
13	US 6402592 B1	11							☑				USPAT
14	US 6390890 B1	36							☑				USPAT

US-PAT-NO: 6402592

DOCUMENT-IDENTIFIER: US 6402592 B1

TITLE: Electrochemical methods for polishing copper films on semiconductor substrates

---------- KWIC ---------

Abstract Text - ABTX (1):

Methods for electrochemically polishing copper films on semiconductor substrates use an alkaline solution with a pH in the range of about 8.0 to 10.5. A constant current density of from 5 to 100 amperes per square foot is applied to an electrochemical cell formed by an electrode, the alkaline solution and the copper film. Copper is removed at a rate of from 500 to 10,000 angstroms per minute. The end point for the electro-polishing is detected by a sudden change in applied voltage. The alkaline polishing solution may also contain copper ions so that when the current direction is reversed, copper is deposited onto the copper film. Furthermore, this copper deposition will occur selectively on the exposed copper surface but not on the exposed barrier layer surface. Hence, the method can compensate for dishing and erosion by re-depositing copper in regions after too much copper was removed from those regions.

TITLE - TI (1):

Electrochemical methods for polishing copper films on semiconductor substrates

Brief Summary Text - BSTX (3):

This invention relates to the field of electrochemical deposition and removal of copper, and, more particularly, to electrochemically polishing copper films.

Brief Summary Text - BSTX (5):

In the manufacture of devices on semiconductor substrates, such as semiconductor wafers, multiple levels of conductive layers are applied to the substrate. In order to fabricate features, circuits, vias and devices on the substrate, various techniques are used to deposit and etch materials on the substrate. Deposition techniques include processes such as physical vapor deposition (PVD), chemical vapor deposition (CVD), and immersion of the substrate into an electrolyte solution. This last technique may be used for either electroless deposition or electroplating.

Brief Summary Text - BSTX (6):

Similarly, a number of techniques are known for removing a material from a wafer. These techniques include wet chemical etching, reactive ion etching (RIE), plasma etching, chemical mechanical polishing (CMP), and immersion of

in form and detail will be within the skill of persons skilled in the art. Therefore, the invention must be measured by the claims and not by the description of the examples or the preferred embodiments.

We claim:

1. A method for polishing a copper film on a semiconductor substrate, comprising the steps of:

(1) immersing the semiconductor substrate having a copper film applied onto at least a portion of a surface thereon into an alkaline solution;

(2) providing a cathode in contact with the alkaline solution that together with the copper film and alkaline solution forms an electrochemical cell; and

(3) applying a current to the electrochemical cell so that a portion of the copper film is removed.

2. The method of claim 1, wherein the alkaline solution contains copper ions as a source of copper for electroplating.

3. The method of claim 1, further comprising, applying a dielectric material to the semiconductor substrate prior to applying a copper film thereon.

4. The method of claim 3, wherein the dielectric material has a low permitivity (K).

5. The method of claim 3, wherein the dielectric material is selected from the group consisting of: silica, SiO_2, F-doped silicate glass, C-doped silicate glass, other doped silicate glasses, polyarylethers, polyimides, polytetrafluoroethylene and carbon polymers.

6. The method of claim 3, wherein the dielectric material is selected from the group consisting of: xerogels, aerogels, porous silicas, porous carbon polymers, porous polyarylethers, and porous polytetrafluoroethylene.

7. The method of claim 1, wherein the current is applied at a density of from 5 to 100 amperes per square foot.

8. The method of claim 7, wherein the current density is from 5 to 30 amperes per square foot.

9. The method of claim 1, wherein the current applied to the electrochemical cell is constant.

10. The method of claim 1, wherein a constant voltage is used in the electrochemical cell.

11. The method of claim 10, further comprising shutting off the voltage after a decrease in current is detected.

12. The method of claim 1, wherein the alkaline solution is maintained at a temperature at or above 70° F.

13. The method of claim 12, wherein the temperature of the alkaline solution is maintained in the range of from room temperature to 150° F.

14. The method of claim 1, wherein the alkaline solution has a pH above 7.

15. The method of claim 14, wherein the alkaline solution has a pH in the range of 8.0 to 10.5.

16. The method of claim 1, wherein the alkaline solution is formed from a mixture of materials selected from the group consisting of copper salts, copper sulfate, copper pyrophosphate, alkali metal pyrophosphates, including sodium pyrophosphate, ammonium pyrophosphate, orthophosphate, sodium hydroxide, potassium hydroxide, ammonium hydroxide and ethylenediaminetetraacetic acid.

17. The method of claim 1, wherein copper is removed at a rate in the range of from 500 to 10,000 angstroms per minute.

18. The method of claim 17, wherein copper is removed at a rate in the range of 1000 to 5000 angstroms per minute.

19. The method of claim 1, further comprising shutting off the current after an increase in applied voltage is detected.

20. A method for alternatively selectively removing copper from and selectively depositing copper onto a copper film on a semiconductor substrate, comprising the steps of:

(1) immersing the semiconductor substrate having a copper film applied to at least a portion of a surface thereon into an alkaline solution;

(2) providing an electrode in contact with the alkaline solution that together with the copper film and alkaline solution forms an electrochemical cell;

(3) applying a current to the electrochemical cell to selectively remove a portion of the copper film; and

(4) optionally applying a reverse current to the electrochemical cell to selectively deposit copper onto the copper film.

21. The method of claim 20, wherein steps (1) to (4) are repeated until a substantially planar surface is formed on the copper film.

22. The method of claim 20, wherein the current is applied at a density of from 5 to 100 amperes per square foot.

23. The method of claim 20, wherein the reverse current is applied at a density of from 5 to 100 amperes per square foot.

24. The method of claim 20, wherein the current applied to the electrochemical cell is constant.

25. The method of claim 20, wherein a constant voltage is used in the electrochemical cell.

26. The method of claim 20, wherein the reverse current applied to the electrochemical cell is constant.

27. The method of claim 20, wherein a constant voltage is used to establish the reverse current.

28. The method of claim 20, wherein the alkaline solution is maintained at a temperature at or above 70° F.

29. The method of claim 28, wherein the temperature of the alkaline solution is maintained in the range of room temperature to 150° F.

30. The method of claim 20, wherein the alkaline solution has a pH above 7.

31. The method of claim 30, wherein the alkaline solution has a pH in the range of 8.5 to 10.5.

32. The method of claim 30, wherein copper is removed at a rate in the range of from 500 to 10,000 angstroms per minute.

33. The method of claim 32, wherein copper is removed at a rate in the range of from 5,000 to 10,000 angstroms per minute.

34. The method of claim 30, wherein copper is deposited at a rate in the range of from 500 to 10,000 angstroms per minute.

35. The method of claim 34, wherein copper is deposited at a rate in the range of from 1,000 to 5,000 angstroms per minute.

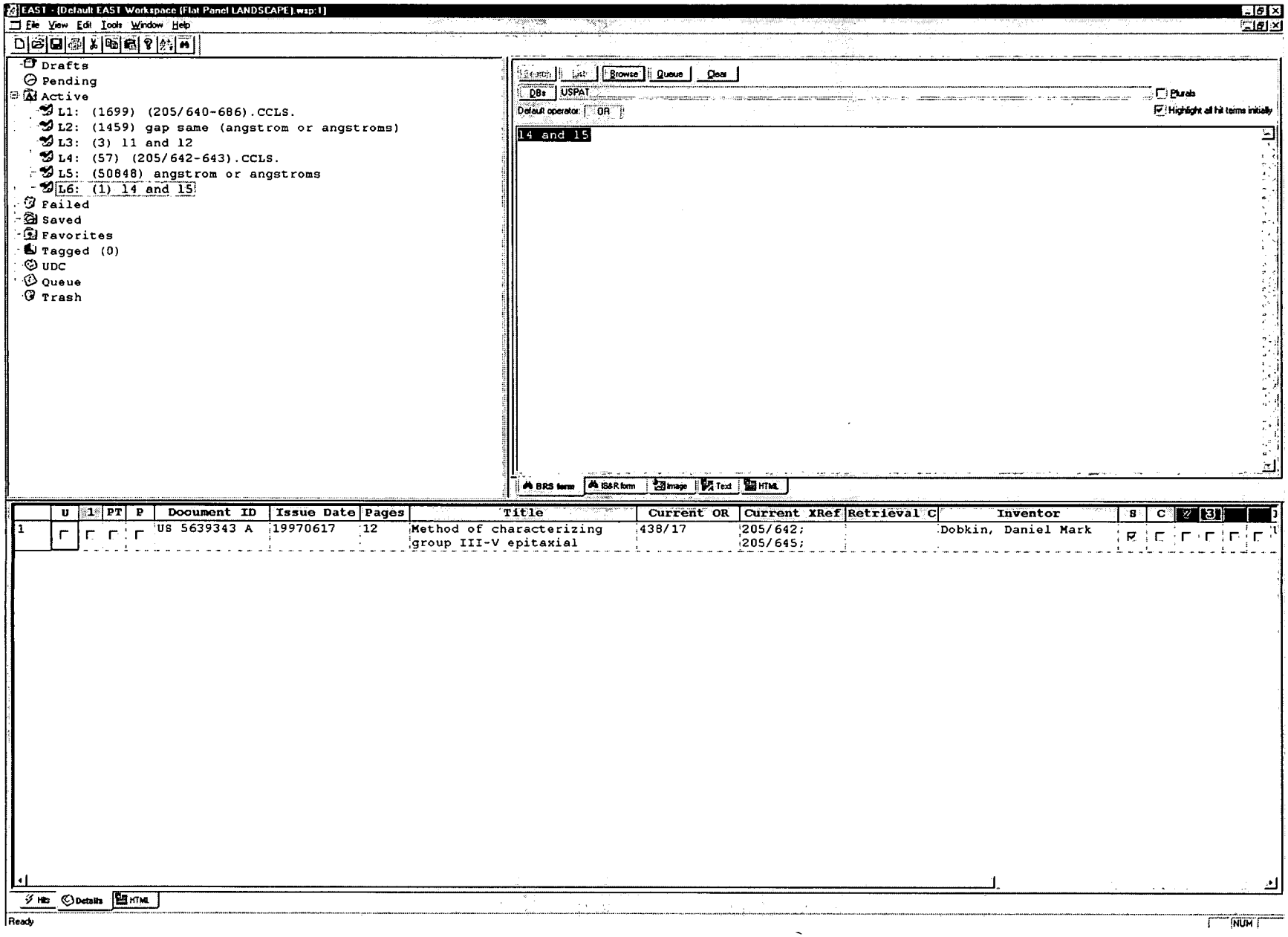
36. The method of claim 30, wherein the alkaline solution is formed from a mixture of materials selected from the group consisting of copper salts, copper sulfate, copper pyrophosphate, alkali metal pyrophosphates, including sodium pyrophosphate, ammonium pyrophosphate, orthophosphate, sodium hydroxide, potassium hydroxide, ammonium hydroxide and ethylenediaminetetraacetic acid.

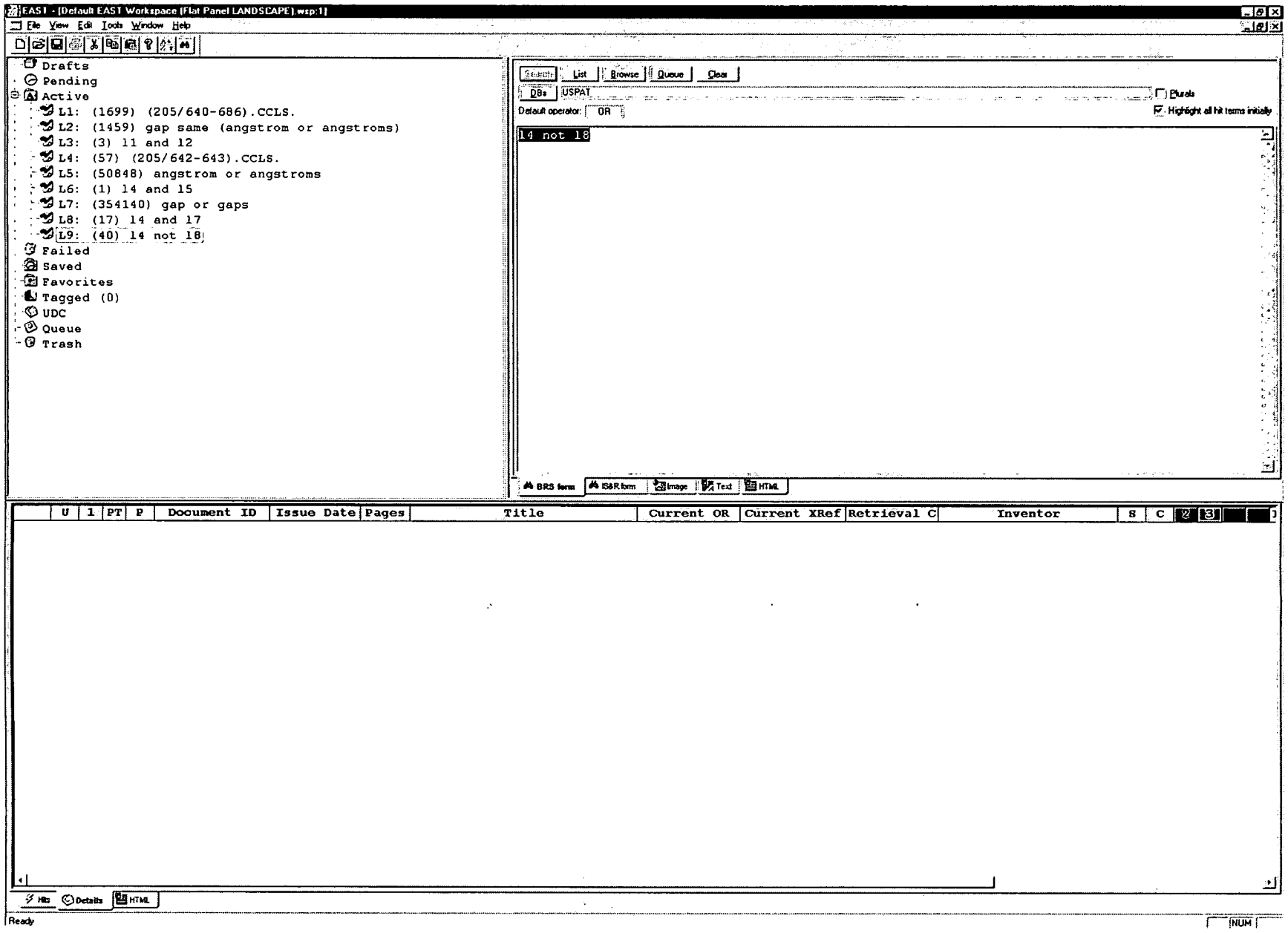
37. The method of claim 30, further comprising shutting off the current after an increase in applied voltage has been detected.

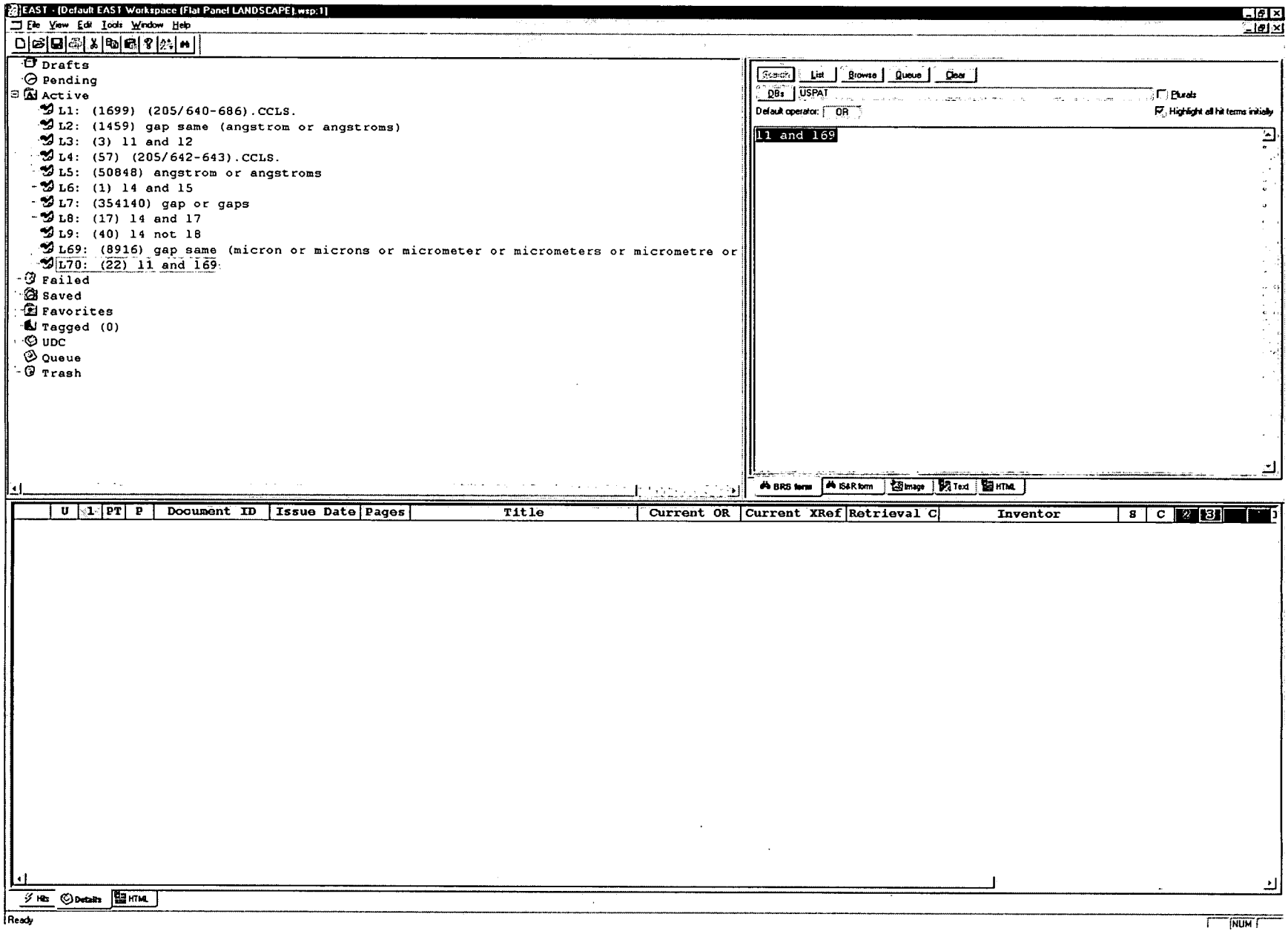
38. The method of claim 30, further comprising shutting off the reverse current after a change in applied voltage has been detected.

39. The method of claim 30, wherein the step of applying a reverse current to the electrochemical cell to selectively deposit copper onto the copper film is carried out after the step of applying a current only if the copper film does not have a substantially planar surface.

* * * * *


EAST - [Default EAST Workspace (Flat Panel LANDSCAPE).wsp:1]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (1699) (205/640-686).CCLS.
L2: (1459) gap same (angstrom or angstroms)
L3: (3) l1 and l2
L4: (57) (205/642-643).CCLS.
L5: (50848) angstrom or angstroms
L6: (1) l4 and l5
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash
Search
List
Browse
Queue
Clear
DBs
USPAT
Default operator:
OR
Plurals
Highlight all hit terms initially
l4 and l5
BRS form
IS&R form
Image
Text
HTML
U
PT
P
Document ID
Issue Date
Pages
Title
Current OR
Current XRef
Retrieval C
Inventor
S
C
1
US 5639343 A
19970617
12
Method of characterizing group III-V epitaxial
438/17
205/642; 205/645;
Dobkin, Daniel Mark
Hits
Details
HTML
Ready
NUM


EAST - [Default EAST Workspace (Flat Panel LANDSCAPE).wsp:1]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (1699) (205/640-686).CCLS.
L2: (1459) gap same (angstrom or angstroms)
L3: (3) l1 and l2
L4: (57) (205/642-643).CCLS.
L5: (50848) angstrom or angstroms
L6: (1) l4 and l5
L7: (354140) gap or gaps
L8: (17) l4 and l7
L9: (40) l4 not l8
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash
Search
List
Browse
Queue
Clear
DBs
USPAT
Default operator:
OR
Plurals
Highlight all hit terms initially
l4 not l8
BRS form
IS&R form
Image
Text
HTML
U
1
PT
P
Document ID
Issue Date
Pages
Title
Current OR
Current XRef
Retrieval C
Inventor
S
C
Hits
Details
HTML
Ready
NUM


EAST - [Default EAST Workspace (Flat Panel LANDSCAPE).wsp:1]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (1699) (205/640-686).CCLS.
L2: (1459) gap same (angstrom or angstroms)
L3: (3) l1 and l2
L4: (57) (205/642-643).CCLS.
L5: (50848) angstrom or angstroms
L6: (1) l4 and l5
L7: (354140) gap or gaps
L8: (17) l4 and l7
L9: (40) l4 not l8
L69: (8916) gap same (micron or microns or micrometer or micrometers or micrometre or
L70: (22) l1 and l69
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash
Search
List
Browse
Queue
Clear
DBs
USPAT
Plurals
Default operator:
OR
Highlight all hit terms initially
l1 and l69
BRS form
IS&R form
Image
Text
HTML
U
PT
P
Document ID
Issue Date
Pages
Title
Current OR
Current XRef
Retrieval C
Inventor
S
C
Hits
Details
HTML
Ready
NUM

EAST Browser - L70: [22] 1 and 69 | US 6214200 B1 | Tag: S | Doc: 4/22 [SORTED] | Format : KWIC

File Edit View Tools Window Help

	Document ID	Pages	1	2	3	.	U	S	C	P	Kind Codes	Sou
1	US 6398942 B1	10						☑				USPAT
2	US 6355156 B1	6						☑				USPAT
3	US 6312584 B1	8						☑				USPAT
4	US 6214200 B1	8						☑				USPAT
5	US 5993638 A	4					☑					USPAT
6	US 5674758 A	42					☑					USPAT
7	US 5641391 A	16					☑					USPAT

US-PAT-NO: 6214200

DOCUMENT-IDENTIFIER: US 6214200 B1

TITLE: Method and arrangement for the electrochemical machining of a workpiece

---------- KWIC ---------

Brief Summary Text - BSTX (19):

The invention is based on the recognition of the fact that moving the electrode and the workpiece away from one another over a desired distance after they have brought into contact does not always result in the desired working distance being set. Owing to a resilient element the resulting working distance may be smaller than the desired working distance and it is even possible that electrical contact persists. The likelihood of this is substantial if the desired working distance is of the order of micrometers . Said resilient element may form part of the arrangement used for positioning the electrode with respect to the workpiece and/or may be formed by a burr or contaminant in the gap . If the working distance is smaller than desired, the current density is higher than intended and there is a large risk of gassing in the gap . As a result of this, there is a large risk of flash-over. If electrical contact persists after the working distance has been set the current density at the location of this electrical contact owing to the operating current will be so high that the electrode and/or the workpiece may be damaged. The measures in accordance with the invention ensure that the actual gap has at least the magnitude of the second distance. This precludes short-circuiting or the generation of a flash-over. As a result of these measures the risk of damaging of the workpiece and/or the electrode is reduced substantially and a working distance of an order of magnitude of micrometers can be set in a reliable manner.

Current US Original Classification - CCOR (1):

205/652

Current US Cross Reference Classification - CCXR (3):

205/654

Current US Cross Reference Classification - CCXR (4):

205/685

Current US Cross Reference Classification - CCXR (5):

205/696

(12) **United States Patent**
Altena et al.

(10) **Patent No.: US 6,214,200 B1**
(45) **Date of Patent: Apr. 10, 2001**

(54) **METHOD AND ARRANGEMENT FOR THE ELECTROCHEMICAL MACHINING OF A WORKPIECE**

(75) Inventors: **Hermanus S. J. Altena; Maarten Brussee; Anton M. Boorsma; Foppe Kramer, all of Drachten (NL)**

(73) Assignee: **U.S. Philips Corporation, New York, NY (US)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/286,115**

(22) Filed: **Apr. 2, 1999**

(30) **Foreign Application Priority Data**

Apr. 6, 1998 (EP) 98201081

(51) Int. Cl.[7] **B23H 3/00; B23H 7/18; B23H 7/32**

(52) U.S. Cl. ..... 205/652; 205/654; 205/685; 205/686; 204/224 M; 204/225

(58) Field of Search ..... 205/652, 654; 204/224 M, 225

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,448,024 * 6/1969 Philpott ..... 205/654 X
4,264,417 4/1981 Vasiliev et al. 204/129.7
6,059,954 * 5/2000 Suda et al. ..... 205/654 X

FOREIGN PATENT DOCUMENTS

1815038A1 5/1993 (SE) .

OTHER PUBLICATIONS

"Modelling and Monitoring Interelectrode Gap in Pulse Electrochemical Machining" by K.P. Rajurkar et al, Annals of the CIRP. vol. 44/1/1995, pp. 177–180.

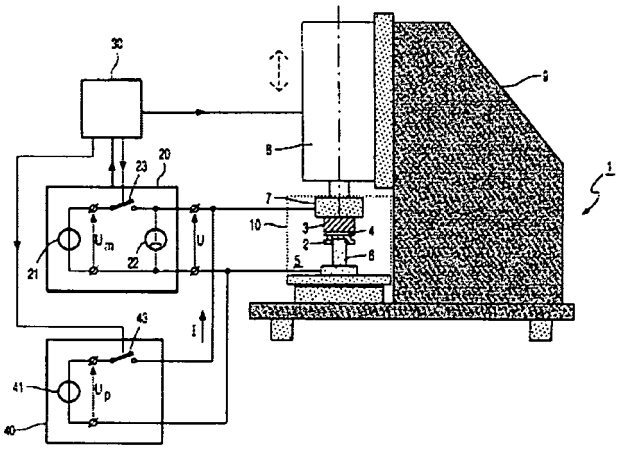
* cited by examiner

Primary Examiner—Donald R. Valentine
(74) *Attorney, Agent, or Firm*—Ernestine C. Bartlett

(57) **ABSTRACT**

In a method for electrochemical machining, the working distance is set by contacting the workpiece with the electrode, increasing the distance between the workpiece and the electrode by a first distance, detecting whether the contact between the electrode and the workpiece is broken, and further increasing the distance between the workpiece and the electrode by a second distance. Owing to this method, very small working distances can be set with a limited risk of short-circuiting and flash-over.

13 Claims, 3 Drawing Sheets



EAST Browser - L8: [17] 4 and 7 | US 3849272 A | Tag: S | Doc: 14/17 (SORTED) | Format: KWIC

File Edit View Tools Window Help

	Document ID	Pages	1	2	3	U	S	C	P	Kind Codes	Sou
9	US 4213834 A	17									USPAT
10	US 4160710 A	9									USPAT
11	US 4134807 A	6									USPAT
12	US 4125444 A	10									USPAT
13	US 3859186 A	14									USPAT
14	US 3849272 A	5									USPAT
15	US 3773636 A	5									USPAT

US-PAT-NO: 3849272

DOCUMENT-IDENTIFIER: US 3849272 A

TITLE: PROCESS FOR EXACT ELECTROCHEMICAL WORKING OF WORKPIECES OF DIFFERENT SHAPE

---------- KWIC ---------

Brief Summary Text - BSTX (3):

The electrochemical working of workpieces of different shape as performed according to actually known methods lacks the required accuracy. An accurate shape of the workpiece corresponding to the shape of the tool is in particular not achieved, if some portion of the worked surface of the workpiece is inclined with respect to the direction of the relative advance of tool and workpiece. When working such inclined objects, a gap corresponding to the condition of equilibrium is created between the tool and the workpiece. This gap achieves different magnitudes, wherein the actual gap between surfaces perpendicular to the advance is smaller than the actual gap between surfaces which are inclined with respect to the relative advance of tool and workpiece. The consequence thereof is, that the tool does not fit exactly into the workpiece after the piece is finished and gaps are always left at the lateral surfaces. In the known techniques, in order to improve the accuracy of working, the magnitude of the working gap has been reduced to the utmost. Even so the required accuracy has not been achieved. In order to achieve an accurate shape of the product, the prior art has resorted to complicated and troublesome corrections of the tool -- and/or of the working electrode. Consequently, the working electrode actually is made with a shape different from that of the finished workpiece. Concomitantly in order to achieve an accurate shape of the product, all of the working parameters for which these corrections have been made must be strictly maintained.

Drawing Description Text - DRTX (7):

FIG. 5 indicates in axial cross section adjustments of a working electrode achieving changes of conductivity of the electrolyte in the working gap .

Detailed Description Text - DETX (2):

Referring to FIG. 1, it will be seen that if it is desired to achieve after completion of working the exact shape in the workpiece of the working tool, the working gap between tool and workpiece at surfaces which are inclined at a certain or determined angle with respect to the direction of relative advance of tool and workpiece must have a certain magnitude with respect to the magnitude of the working gap of surfaces which are perpendicular to this direction, namely

Detailed Description Text - DETX (5):

d.sub.b is the lateral working gap of a surface inclined with respect to the direction of advance

United States Patent [19]

Zubak

[11] 3,849,272

[45] Nov. 19, 1974

[54] PROCESS FOR EXACT ELECTROCHEMICAL WORKING OF WORKPIECES OF DIFFERENT SHAPE

[75] Inventor: Jan Zubak, Ostrov, Czechoslovakia

[73] Assignee: Vyskumny ustav Automatizacie a mechanizacie, Nove Mesto nad Vahom, Czechoslovakia

[22] Filed: Oct. 15, 1971

[21] Appl. No.: 189,634

[30] Foreign Application Priority Data

Dec. 8, 1970 Czechoslovakia 8247/70

[52] U.S. Cl. ..... 204/129.25, 204/224 M

[51] Int. Cl. B23p 1/14, B23p 1/04

[58] Field of Search 204/129.1, 129.2, 129.25, 204/129.5, 129.55

[56] References Cited

UNITED STATES PATENTS

3,075,902	1/1963	Bradley et al.	204/129.2
3,372,099	3/1968	Clifford	204/129.2
3,580,827	5/1971	Lannegrace	204/129.25
3,630,878	12/1971	Haggerty	204/225

FOREIGN PATENTS OR APPLICATIONS

42-17414	9/1967	Japan	204/129.25

OTHER PUBLICATIONS

Electrochemical Machining by De Barr et al., pp. 158, 159, Pub. by American Elseview, New York, 1968.

Electrochemical Machining by De Barr et al., pp. 61–67, pub. by American Elsevier Pub. Co., New York, 1968.

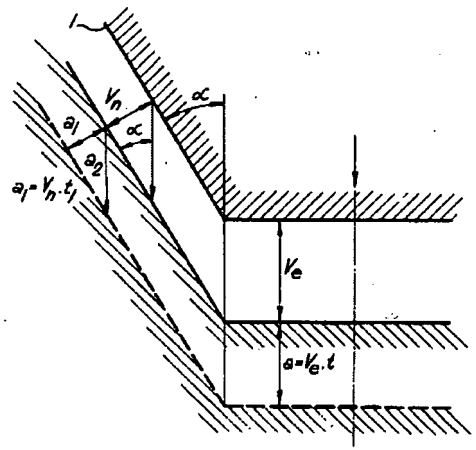
Primary Examiner—F. C. Edmundson

Attorney, Agent, or Firm—Murray Schaffer

[57] ABSTRACT

Working of workpieces by the electrochemical method, which workpieces have surfaces inclined with respect to the direction of relative advance of tool to workpiece. At least one of the working parameters, such as voltage, conductivity of the electrolyte, surface of electrode, and/or time of working is adjusted with respect to the parameter applied for working of surfaces perpendicular to the direction of relative advance of tool and workpiece.

6 Claims, 5 Drawing Figures



EAST Browser - L9: [40] 4 not 8 | US 5096550 A | Tag: S | Doc: 7/40 (SORTED) | Format : KWIC

File Edit View Tools Window Help

	Document ID	Pages	1	2	3	U	S	C	P	Kind Codes	Sou
2	US 5385652 A	7					☑				USPAT
3	US 5338416 A	14					☑				USPAT
4	US 5336379 A	7					☑				USPAT
5	US 5112453 A	15					☑				USPAT
6	US 5102520 A	11					☑				USPAT
7	US 5096550 A	12					☑				USPAT
8	US 4891103 A	19				☑					USPAT

US-PAT-NO: 5096550

DOCUMENT-IDENTIFIER: US 5096550 A

TITLE: Method and apparatus for spatially uniform electropolishing and electrolytic etching

---------- KWIC ----------

Current US Original Classification - CCOR (1):

205/642

US005096550A

United States Patent [19]

Mayer et al.

[11] Patent Number: 5,096,550

[45] Date of Patent: Mar. 17, 1992

[54] METHOD AND APPARATUS FOR SPATIALLY UNIFORM ELECTROPOLISHING AND ELECTROLYTIC ETCHING

[75] Inventors: Steven T. Mayer, Piedmont; Robert J. Contolini, Pleasanton; Anthony F. Bernhardt, Berkeley, all of Calif.

[73] Assignee: The United States of America as represented by the United States Department of Energy, Washington, D.C.

[21] Appl. No.: 597,225

[22] Filed: Oct. 15, 1990

[51] Int. Cl.[5] C25F 3/02; C25F 3/16; C25F 7/00

[52] U.S. Cl. 204/129.1; 204/129.25; 204/129.2; 204/212; 204/228; 204/231; 204/237; 204/238; 204/239; 204/240; 204/252; 204/DIG. 7

[58] Field of Search ..... 204/129.1, 129.65, 129.7, 204/212, 224 M, 231, 228, 252, 263-266, 237-238, 241, 273, 297 R, DIG. 7

[56] References Cited

U.S. PATENT DOCUMENTS

3,692,639	9/1972	Delmouzos	204/DIG. 7
3,703,458	11/1972	Read et al.	204/252 X
3,849,270	11/1974	Takagi et al.	204/129.1
4,073,708	2/1978	Hicks, Jr.	204/252 X
4,238,310	12/1980	Eckler et al.	204/252
4,971,676	11/1990	Doue et al.	204/297 R

OTHER PUBLICATIONS

"Electropolishing of Vertical Copper Cylinders in Phosphoric Acid Under Natural Convention Conditions" by G. H. Sedahmed et al., *Surface Technology*, 11, pp. 67-71 (1980).

"Electropolishing" article in *McGraw-Hill Encyclopedia of Science & Technology*, pp. 810-811 (1982).

Primary Examiner—Donald R. Valentine

Attorney, Agent, or Firm—Henry P. Sartorio; L. E. Carnahan; William R. Moser

[57] ABSTRACT

In an electropolishing or electrolytic etching apparatus the anode is separated from the cathode to prevent bubble transport to the anode and to produce a uniform current distribution at the anode by means of a solid nonconducting anode-cathode barrier. The anode extends into the top of the barrier and the cathode is outside the barrier. A virtual cathode hole formed in the bottom of the barrier below the level of the cathode permits current flow while preventing bubble transport. The anode is rotatable and oriented horizontally facing down. An extended anode is formed by mounting the workpiece in a holder which extends the electropolishing or etching area beyond the edge of the workpiece to reduce edge effects at the workpiece. A reference electrode controls cell voltage. Endpoint detection and current shut-off stop polishing. Spatially uniform polishing or etching can be rapidly performed.

42 Claims, 5 Drawing Sheets